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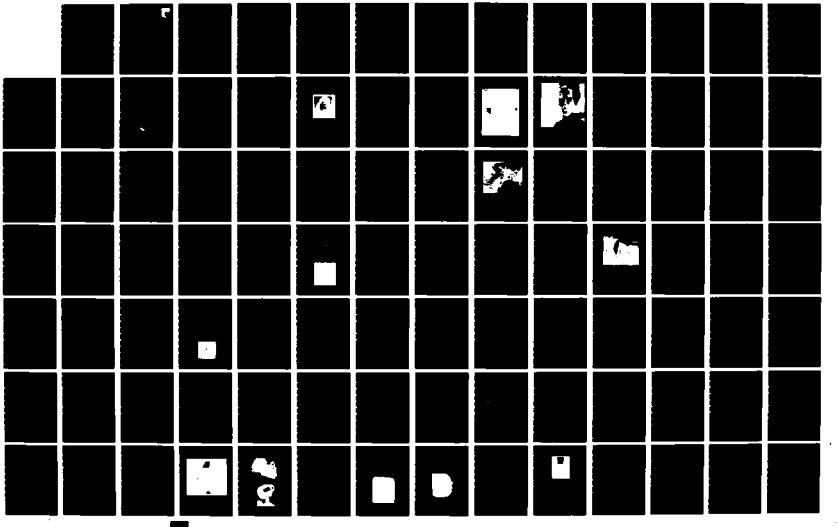

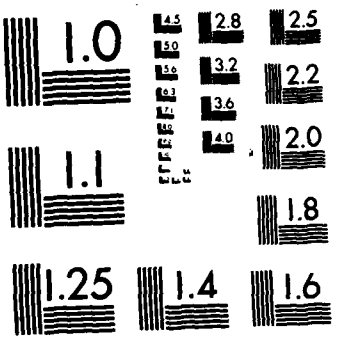

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HEAD-UP DISPLAY (HUD) TECHNOLOGY DEMONSTRATION

J. E. Gunther
Hughes Aircraft Company
Display Technology Staff
Display Systems Laboratory
El Segundo, California 90245

JULY 1983
Final Report for Period 15 April 1980 – 30 March 1983

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The objectives of the Head-Up Display Technology Demonstration program were to demonstrate the feasibility of constructing liquid crystal matrix display modules with high optical performance and few defective elements, and of using optical projection techniques to combine the images from multiple, physically separate, display modules into a continuous high resolution display surface.

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Most of the original objectives of Head-Up Display Technology Demonstration program have been achieved or exceeded. Major improvements in display brightness and contrast have resulted from the development of improved matrix smoothing techniques and specular projection systems, and from the incorporation of low reflectivity transparent electrodes. The 60% reflectivity and greater than 30:1 contrast of the liquid crystal modules produced on this program are adequate to meet all known projection display requirements.

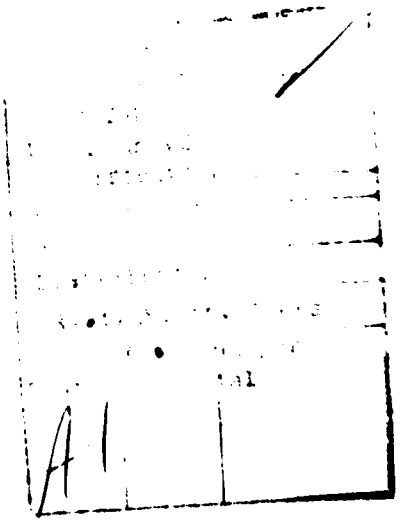
The most significant accomplishment of the efforts on the Head-Up Display Technology Demonstration program was the demonstration of the feasibility of using projection techniques to combiner the images from multiple display modules. A 350 x 350-element, 7 x 7-inch, 4-module projection display with an average raster brightness of 3800 foot lamberts was demonstrated. This development may lead to a truly modular display architecture in which a single type of display module can be replicated and stacked to produce displays with high brightness and contrast and arbitrarily high resolution.

PREFACE

The completion of the Head-Up Display Technology Demonstration program was the result of an interdisciplinary team effort by individuals from four separate areas of Hughes Aircraft Company. The Display Systems Laboratory, Radar Systems Group, provided overall program management, project and system engineering, and design staff for electronic and mechanical tasks. The Liquid Crystal Products area of the the Industrial Electronics Group was responsible for the fabrication of the liquid crystal matrix display modules and the associated LSI drivers. The Chemistry Section of the Hughes Research Laboratory formulated the liquid crystal material and consulted on display assembly issues. The Optics Section, Missile Systems Group, performed the design of the custom projection optics.

The team of individuals whose efforts contributed to the completion of the Head-Up Display Technology Demonstration program included: R. Bernstein, M. Ernstoff, J. Ferrer, J. Gunther, R. Hegg, W. Hoffman, and M. Lund of the Radar Systems Group; W. Bleha, B. Fletcher, R. Lloyd, D. Murillo, and S. Shields of the Industrial Electronics Group; A. Lackner and J. Margerum of the Hughes Research Laboratories; and R. Fischer and R. Murray of the Missile Systems Group. Silicon processing was performed by the Industrial Products Division MOS Laboratory under the direction of J. Mintz and by the Industrial Electronics Group Carlsbad Research Center under the direction of K. Mar.

The program was monitored and directed for the Air Force by John Coonrod. James Skalski of the Air Force provided significant consultation services in the area of integrated circuit processing.



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SECTION I.

INTRODUCTION AND SUMMARY

1. BACKGROUND

The complexity of modern military weapons, communications, and sensor systems has increased the need for electronic displays in airborne applications. While most current display requirements are satisfied by cathode ray tube (CRT) displays, an alternative display technology must be developed to provide the higher brightness, contrast, resolution, and reliability that will be required in future aircraft. The Head-Up Display is one specific application in which an alternative display technology could provide significant improvements in reliability, performance, and cost.

The Head-Up Display (HUD) is an optically projected display which forms a collimated image. This image is reflected from a combining glass located in the pilot's forward field of view. The combining glass also transmits the real world scene such that the pilot sees the display and real-world images superimposed. Since the displayed symbology is often viewed against a bright background, the symbol brightness required in HUD's taxes the capabilities of current CRT technology. Current HUD's are characterized by high cost, high power consumption, and very low reliability. The typical Mean Times Between Failures (MTBF's) of current HUD's range from 50 to 125 hours.

The A-7D, A-10, F-14, F-15, F-16, and F-18 aircraft currently carry HUD's. These displays are used to present digitally generated vector-graphic symbol cues for take-off, landing, flight control, navigation, terrain following/avoidance, and, primarily, weapons delivery. HUD systems now being developed also present Forward Looking Infrared (FLIR) information, in raster format, for navigation and targeting.

Instrument panel space will be reduced in future tactical aircraft due to reduced aircraft profiles and Hi-G configurations. Thus the dependence on the head-up display will be increased. Since HUD's will be used as primary flight instruments in future aircraft, significant improvements over current technology are required. The Field of View (FOV) of future HUD's will be enlarged through the use of diffraction optics technology. The resolution of the image source within the HUD must be increased in proportion to the increase in FOV. The brightness and contrast of HUD's must be significantly improved to provide the capability to present sensor information, such as FLIR imagery, in a daylight ambient. Most importantly, the reliability of future HUD's must be greatly increased.

In recognition of the need for improved cockpit displays, Hughes Aircraft began investigating advanced display technologies in 1971. Since Hughes is involved in the development and production of airborne radar and infrared sensors, weapons control systems, and wide-field-of-view Head-Up displays, the goal of this advanced display investigation was to select a technology which had the potential to satisfy most cockpit display requirements, including the high resolution wide dynamic range video displays that will be required by future sensor systems.

Our investigation of advanced display technologies resulted in three major conclusions. First, we concluded that none of the light-emitting display technologies (electroluminescent, light emitting diode, gas discharge, or even cathode ray tube) will be able to simultaneously provide the brightness, contrast, and resolution required to present future sensor video information under the high ambient illumination found in many military cockpits. Second, we concluded that liquid crystals were the only nonemissive display technology with the potential to satisfy the majority of cockpit display requirements. Finally, we concluded that, without the use of active circuit elements at each display pixel, the characteristics of the liquid crystal materials and external drive electronics would unacceptably limit the resolution of displays using simple multiplexed addressing techniques.

Thus the advanced display approach being developed at Hughes Aircraft is to sandwich a layer of liquid crystal material between a cover glass coated with a transparent electrode and a silicon matrix addressing circuit chip, as illustrated in Figure 1. The chip contains an X-Y matrix array of reflective electrodes that define the display elements, a switching transistor and storage capacitor for each element, and row and column bus electrodes. The column busses connect to the drains of the transistors at each element in their respective columns. Similarly, each row electrode connects to the gate of every transistor in the corresponding row.

A line-at-a-time addressing technique, similar to that used on other matrix displays, is used to create the images on the display. To write one line, voltages corresponding to the desired response of each element are placed on the column electrodes. A voltage pulse is applied to the appropriate row electrode, the transistors in the row conduct, and each elemental storage capacitor charges to the voltage applied to the corresponding column electrode. The storage capacitors hold the energy required to energize the liquid crystal material until the row is rewritten during periodic refresh. This addressing approach avoids the half-select and duty cycle problems which limit the resolution of liquid crystal displays using multiplexed addressing.

The liquid crystal material selected for use in the Hughes matrix liquid crystal display devices is a dynamic scattering material designed for long life under direct current (DC) operation. This material was chosen because it is compatible with MOS circuitry and has the speed and grey shade capability to provide real-time video images.

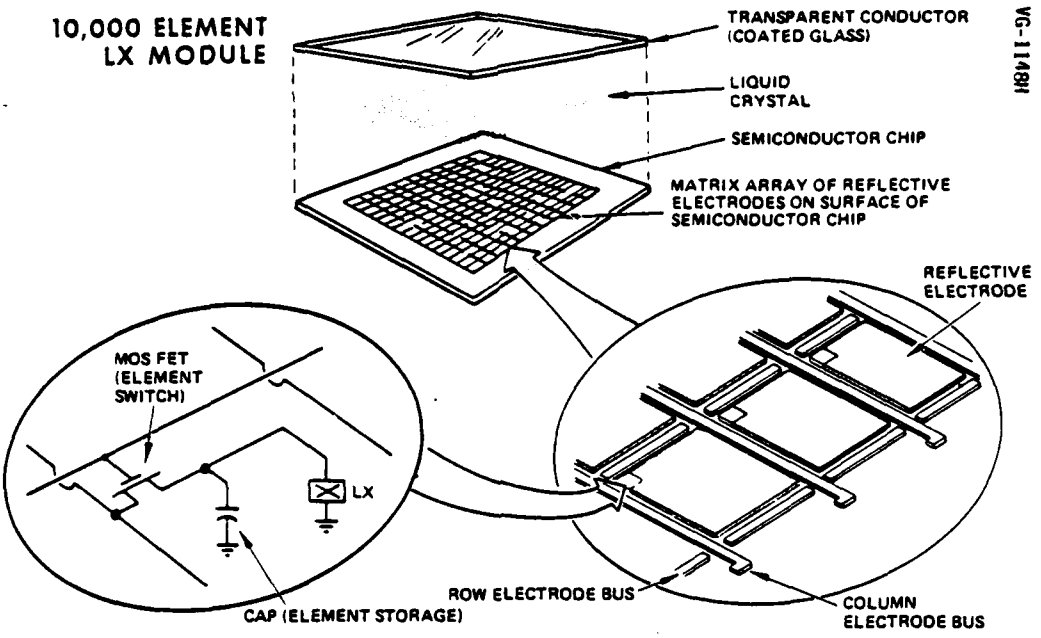


Figure 1. Liquid crystal matrix display construction.

The dynamic scattering electro-optical effect functions by varying the angular distribution of light reflected from the display module. With no voltage applied to the liquid crystal layer, the material is clear, and incident light is specularly reflected. With a voltage applied, the liquid crystal material becomes turbulent and scatters the reflected ambient light. This effect provides high contrast in conjunction with a projection system, as shown in Figure 2.

In this projection system, light which is specularly reflected from unenergized elements passes through an aperture and is projected as bright areas on the screen. On the other hand, the great majority of the light scattered by energized elements is blocked by the aperture plate; the corresponding areas on the screen appear dark.

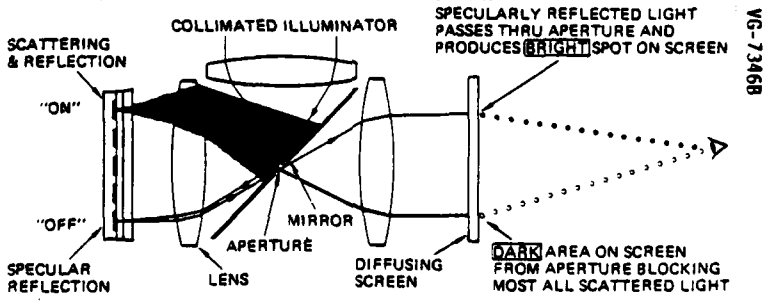


Figure 2. Basic liquid crystal projection display system.

The first 100x100-element, one inch square, liquid crystal matrix display was demonstrated in September 1973. The one inch square format was the largest size that could be constructed using two-inch diameter silicon wafers. The first defect free device of this type was completed in June of 1975. In recognition of the need for a larger display with higher resolution, a two inch square "quad" display, constructed from four edge-abutted one inch chips, was demonstrated in December of the same year.

In 1976, a transition was made to three-inch silicon wafer processing, and the design of the 175x175 element, 1.75-inch square matrix display was begun. The first of these devices was completed in mid 1977, roughly 2.5 years before the start of this program. This display design was developed and refined on a previous program, "Study and Development of an Integrated Head-Up Display", Contract F33615-76-1243.

The results of the Integrated Head-Up Display program demonstrated that the combination of matrix liquid crystal and rear projection technologies can provide a HUD with brightness and contrast, against high outside scene brightness levels, far surpassing those of current HUD's using CRT devices. These same technologies can also be used to construct monochromatic and multi-color head-down displays with significantly improved performance over CRT displays in high ambient illumination levels. However, the current liquid crystal matrix display technology cannot provide, within a single liquid crystal module, the resolution required for many cockpit display applications.

Several 3.5-inch square, 350x350-element, "quad" displays were fabricated during the Integrated Head-Up Display Program, all of which exhibited many line defects during assembly. These "quad" displays consisted of four physically adjacent 175x175-element liquid crystal matrix displays. The problems encountered in fabricating these "physical quads" provided the incentive to develop, as part of the Head-Up Display Technology Demonstration program, a method for combining the images from four separately-tested, physically-independent, matrix display modules.

2. SUMMARY OF ACCOMPLISHMENTS

The Head-Up Display Technology Demonstration program was performed under contract number F33615-79-C-1887 with the objectives of demonstrating the feasibility of constructing liquid crystal matrix display modules with high optical performance and few defective elements, and of using optical projection techniques to combine the images from multiple, physically separate, display modules into a continuous high resolution display surface.

The first objective of the Head-Up Display Technology Demonstration program was to improve the electro-optical performance of the liquid crystal display devices by various techniques such as the use of redundant drive, reduction of defects during processing, improved smoothing techniques, and improved wafer testing procedures. The vehicle for the development of these techniques was the 175x175-element, 1.75-inch square, matrix display module originally developed on the predecessor Integrated Head-Up Display program.

The 175x175-element module was selected because it provided a well defined starting point for the efforts on this program, and because it avoided the technical risk and cost associated with the development of a completely new display device.

Significant progress was made in improving the electro-optical performance of the 175x175-element display module. Wafer testing procedures were improved to include detection of shorts between adjacent lines and between rows and columns of the display matrix. Numerous wafer processing experiments were performed, and the number of line defects was decreased through a combination of improved processes and the use of one experienced processing technician to perform all process steps on a given lot of wafers. Defects in the silicon matrix were further reduced by a defect correction process that converts shorted row and column buses into open circuits. These open rows and columns then function normally when driven redundantly (drive signals are applied to each end of the open row or column). Several displays were fabricated without line defects, and the typical display fabricated near the end of this program had only a few line defects.

The contrast and reflectivity of the display modules was improved by a surface smoothing process, originally developed prior to the start of this program on a company-sponsored effort and refined and implemented during the Head-Up Display Technology Demonstration program. A second-generation version of this process was developed which nearly eliminates defects during the smoothing operation. Additional contrast improvements were obtained by incorporating a multi-layer transparent electrode which has much lower reflectivity than the single-layer electrode previously used. The display modules produced near the end of this program had specular reflectivities above 60% and contrast ratios above 30:1 in a simulated projection system. A video image on one of the displays fabricated on this program is shown in Figure 3.

In a separate tri-service-sponsored effort, a 240x320-element, 321 element per inch, high density module was developed on the Miniature Flat Panel Display program, under contract DAAK-70-77-C-0225) with the Army Night Vision and Electro-Optics Laboratory, in parallel with the first half of the Head-Up Display Technology Demonstration program.

In the future, the high density display module will be used to construct projection displays systems that provide higher resolution and more compact size than systems constructed using the 175x175-element device. Many of the performance improvement techniques developed on the Head-Up Display Technology Demonstration program have been transferred to the high density module on a separate, company sponsored, effort.

The second major objective of the Head-Up Display Technology Demonstration program was to develop a projection optical system which would provide high display brightness and contrast and the capability to combine the images from multiple, physically-separate, display modules. The starting point for this effort was the specular-mode projection system that had been developed on the predecessor Integrated Head-Up Display program. In the

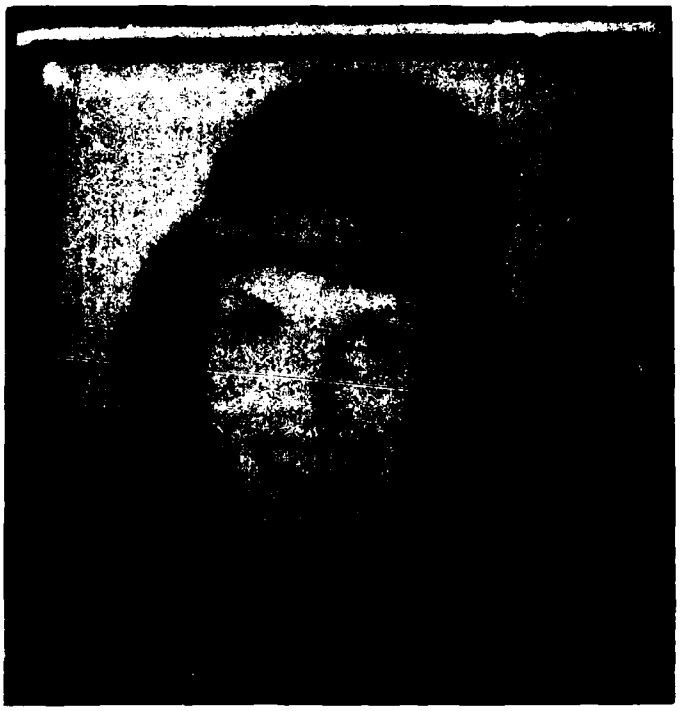


Figure 3. Video image on typical 175x175-element display module.

specular-mode projector, the bright areas on the viewing screen are caused by light that has been specularly reflected from "off" (no voltage applied) areas on the liquid crystal matrix display module. Dark areas on the screen are produced by applying voltage to the liquid crystal material which then scatters the incident light away from a small aperture in the projection optical system.

The concept of using the specular reflections from the liquid crystal module to form the bright areas on the screen offers high optical efficiency and high display brightness and the capability for very high contrast. However, the specular-mode projector implemented in the Integrated Head-Up Display program used an ellipsoidal reflector to collect the light from the lamp source, which caused nonuniform illumination of the liquid crystal module, and an off-axis projection lens which resulted in distortion in the projected image. To improve on this design, a trade-off study was performed on alternative projection techniques, subject to the conditions that

refractive optics (glass lenses) be used to collected the light from the illumination source to provide uniform illumination and that nearly on-axis projection optics would be used to minimize distortion.

Two alternative approaches to constructing a four-module projection display were identified. The first was to use mirrors to combine the images from the four liquid crystal modules prior to projection through a single lens. This approach has the advantage that the four images are combined before any distortion is introduced by the projection lens, and nearly perfect registration is assured. This "single lens" approach had two significant disadvantages -- the mechanical structure of the four-module display is complex and difficult to fabricate on an optical bench, and the concept cannot be extended to displays using more than four modules.

The second approach was to use one projection lens for each liquid crystal module and to combine the projected images on a common screen. This approach is mechanically simple, but extremely low distortion projection lenses are required if the images are to be combined without objectionable discontinuities. This approach has the significant advantage that, assuming suitable projection lenses, more than four liquid crystal/projection lens modules can be combined to produce display of high resolution. Since future wide field of view HUD's may require 700x1000-elements, the ability to combine six or more modules is very desirable, and the lens-per-module approach was selected for development.

The basic design of a single module of the final four module projection system is illustrated in Figure 4. The condensing optics form an image of the lamp arc in front of the projection lens. The projection lens collimates the incoming light and then reforms the image of the arc at the aperture after the light is reflected from the liquid crystal module. Unenergized areas on the liquid crystal module produce bright areas on the projection screen, since most of the reflected light passes through the aperture. Energized, scattering, areas on the module produce dark areas on the screen since only a small fraction of the reflected light passes through the aperture.

The projection lens in this system must be optimized to perform two functions. It must form a low distortion projected image of the liquid crystal module, and it must also form an image of the lamp arc at the aperture with minimal aberrations.

A total of four low distortion projection lens designs were completed. The first was designed for a relative aperture, or speed, of f/1.0 to minimize the length of the projection system. However, the distortion produced by this lens was well above the objective of less than 10% of a picture element. The second design was also an f/1.0 lens which used two additional elements to reduce distortion. However, these lenses would not mechanically fit into the optical bench projection system. The third design had a speed of f/2.0 and essentially no distortion. We attempted to find an optimum compromise between distortion and projection systems length by using a fourth design . This design had a speed of f/1.4 which resulted in acceptably small distortion and an optical path length of 14 inches.

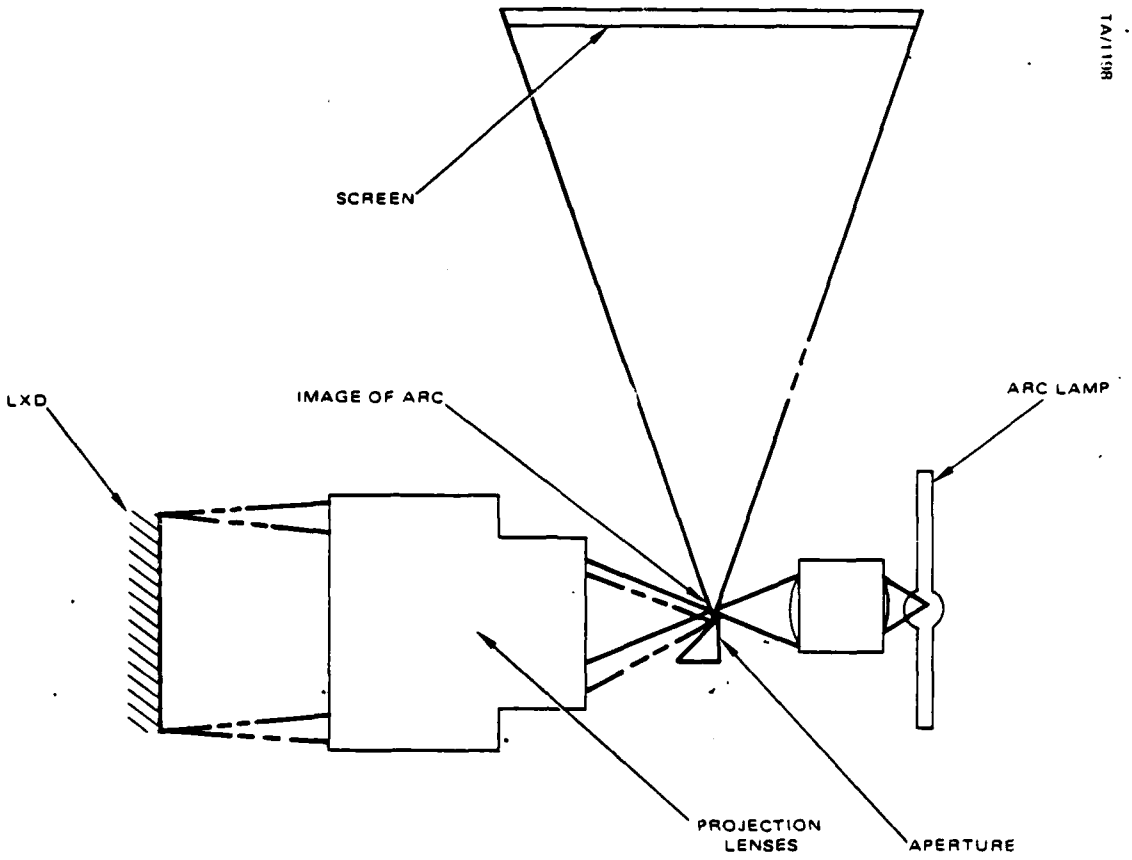


Figure 4. Functional design of a single module projector.

Four f/1.4 projection lenses were fabricated and a functional model of the four module projection system was constructed on an optical bench using standard bench fixtures. This model, shown in Figure 5, presented 350x350 elements on a seven by seven inches screen. For convenience in construction, the model was constructed with the major optical axis perpendicular to the optical bench. The screen is at the top of the model, parallel to the bench, and is viewed through a 45-degree mirror above the screen.

Suitable interface and drive electronics was constructed to allow presentation of real-time video images on the 350x350-element four module projection display. An example of this imagery is shown in Figure 6. The junctions of the four quadrants of the display are perceptible but no information is lost at these junctions. The uniformity of the display is good, and the brightness and contrast are far beyond those achievable over this screen area with any other known display technology. The performance of the four module display is summarized in Table 1.

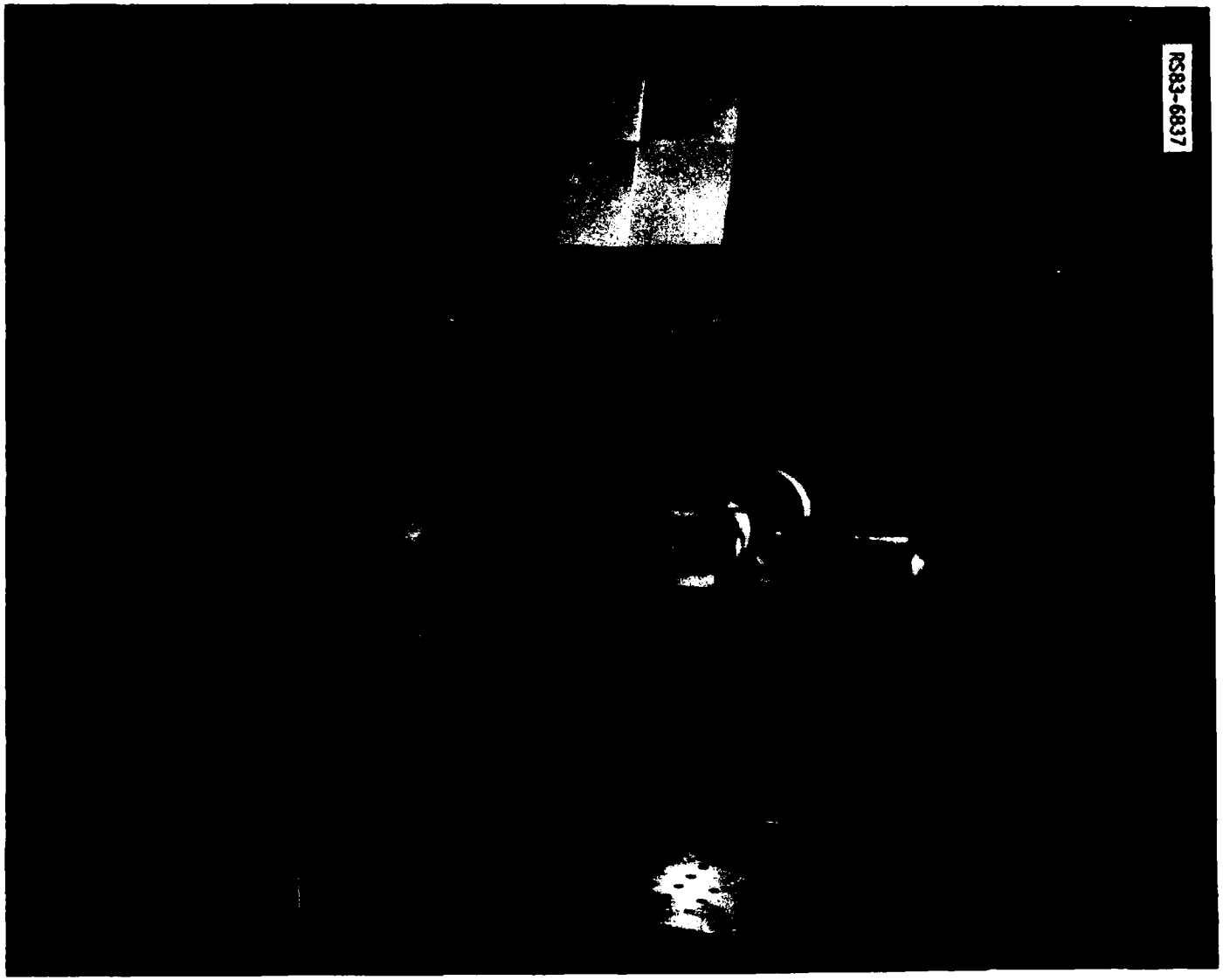


Figure 5. Optical bench model of a four module projection display.

Figure 6. Video image on the 350x350-element four module projection display.

Most of the original objectives of Head-Up Display Technology Demonstration program have been achieved or exceeded. Major improvements in display brightness and contrast have resulted from the development of improved matrix smoothing techniques and specular projection systems, and from the incorporation of low reflectivity transparent electrodes. The 60% reflectivity and greater than 30:1 contrast of the liquid crystal modules produced on this program are adequate to meet all known projection display requirements.

TABLE 1.

FOUR MODULE PROJECTION DISPLAY PERFORMANCE SUMMARY

Viewing Screen Size, inches	7x7
Resolution, elements	350x350
Lamp Power, watts	100
Brightness, foot-Lamberts	
Upper Left Quadrant	3900
Upper Right	4000
Lower Left	3500
Lower Right	4100
Contrast Ratio, No Ambient	
Upper left	17
Upper Right	11
Lower Left	18
Lower Right	17

Although the efforts on this program did not result in a large number of defect-free 175x175-element liquid crystal display modules, improvements in wafer processing, testing, and defect correction did result in a significant decrease in the number of defects. These improvements will assure high yields of the smaller, easier to fabricate, 240x320-element high density display module that will be used in future development efforts.

The most significant accomplishment of the efforts on the Head-Up Display Technology Demonstration program was the demonstration of the feasibility of using projection techniques to combine the images from multiple display modules. This development may lead to a truly modular display architecture in which a single type of display module can be replicated and stacked to produce displays with high brightness and contrast and arbitrarily high resolution.

The next section will discuss the silicon circuit processing used to fabricate the display matrix circuit through the first electrical test point. The processes used to correct defects and to impart the desired optical properties to the matrix circuit are considered proprietary by Hughes and will be not described in this report. The assembly of the matrix circuits into liquid crystal display devices is discussed in Section III. Sections IV. and V. describe the design, construction, and evaluation of the optical bench model four-module projection display. The final section summarizes the conclusions of this effort and makes recommendations for further development.

SECTION II.

SILICON MATRIX CIRCUIT PROCESSING

1. INTRODUCTION

The fabrication of a 175x715-element liquid crystal matrix display proceeds through three distinct phases. The first phase is the relatively conventional Metal-Oxide-Semiconductor (MOS) integrated circuit processing used to construct the matrix circuit through the polysilicon level. This phase, including the electrical tests of the silicon wafers after patterning of the polysilicon level, will be described in this section. The next phase is the unique processes which are used to complete the matrix circuit. These processes are considered propietary by Hughes and are not discussed in this report. The third phase in the construction of a liquid crystal matrix display is the assembly of the matrix circuit into an actual display device. These process steps, beginning with sawing the chip from the silicon wafer and ending with the test of the completed display, will be discussed in Section III. of this report.

The basic MOS integrated circuit process steps used to fabricate the matrix circuit are depicted in Figure 7. Virgin 3-inch-diameter, (1-0-0) orientation, 3-5 ohm-centimeter, n-type silicon wafers are initially oxidized. The source/drain regions are defined by etching openings in the oxide layer, through which boron is diffused. The wafers are re-oxidized and openings corresponding to the channel stop regions are etched in the oxide and the regions are implanted with phosphorous. The implant is activated and redistributed during the subsequent growth of the field oxide.

Openings are etched in the field oxide corresponding to both the gate oxide and contact regions. The gate oxide is grown, and the contact holes to the source/drain diffusions are opened. Boron-doped polysilicon is then deposited by Low Pressure Chemical Vapor Deposition (LPCVD) and etched into the desired electrode patterns. At this point the wafers are electrically tested for shorts and opens on each of the 175 drain and 175 gate bus electrodes. This testing completes the first phase of the display fabrication process.

After test, the wafers having ten or fewer defective lines are continued on to the next phase of the process. The second phase includes proprietary processes for the location and, in some cases, correction of the defects, deposition of optical-quality reflective electrodes at each picture element, and additional electrical and optical tests. After completion of these process steps, the wafers are assembled into displays as described in Section III.

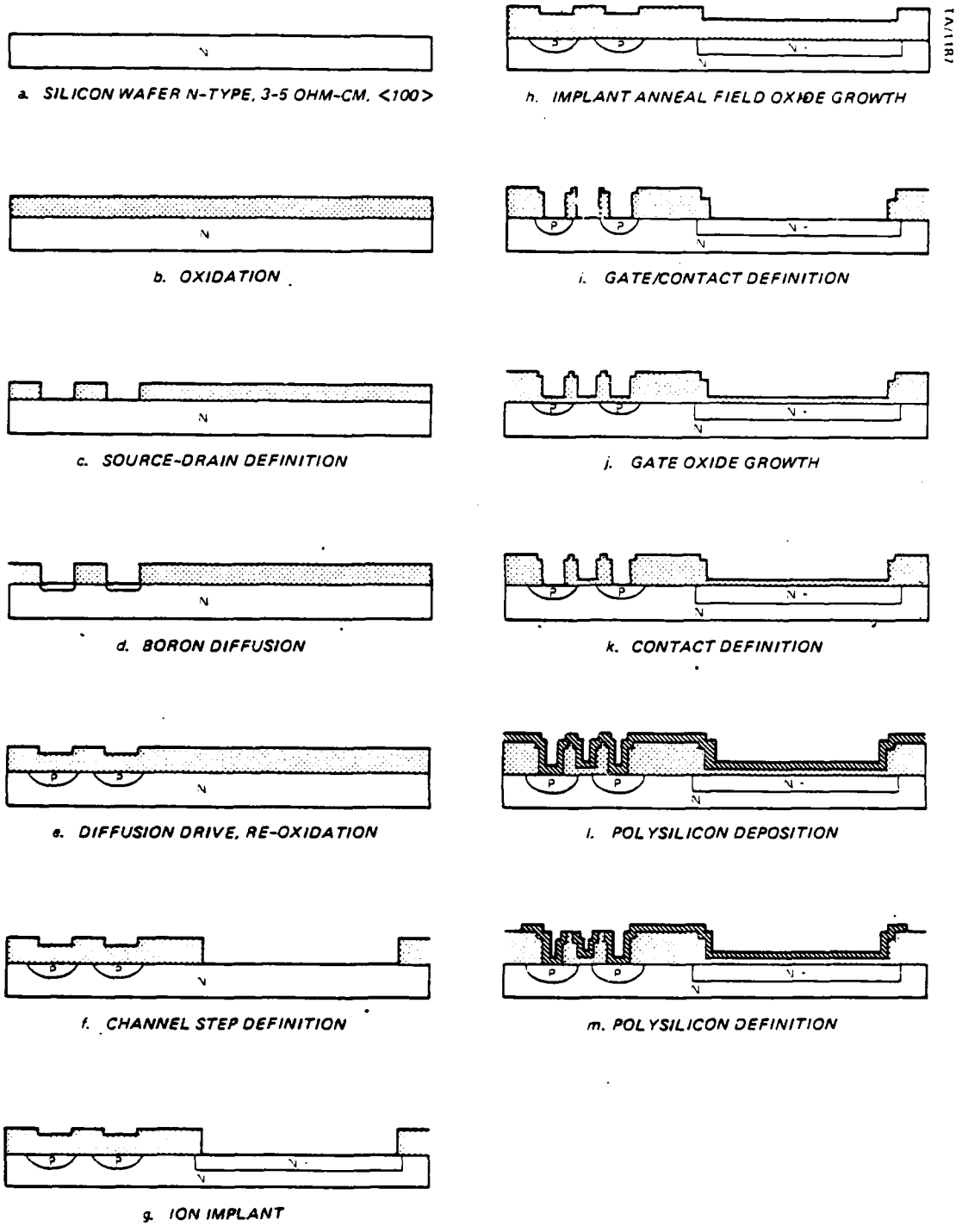


Figure 7. Pictorial diagram of the MOS integrated circuit processing sequence.

2. PROCESS EXPERIMENTS

At the start of the current program, the baseline MOS processing sequence was the same as that used on the predecessor Integrated Head-Up Display Program. During the course of the current program, numerous process improvement tests were performed. These tests are summarized in Table 2, and the results of each test are described in the following paragraphs.

Wafer Back-Grinding

Since precise control of wafer thickness was required on the predecessor Integrated Head-Up Display program, the backs of the wafers used on that program were ground until all wafers had a common thickness. The grinding process resulted in a large amount of powdered silicon which adhered to the grinding marks on the back of the wafer. This powdered silicon could not be removed until the hydrofluoric acid etch after the initial oxidation, at which time clouds of silicon powder were released into the etching solution.

TABLE 2.

SUMMARY OF PROCESS VARIATIONS AND EXPERIMENTS

1.	Elimination of grinding of the wafer backs.
2.	Increased gate oxide thickness.
3.	Increased field oxide thickness.
4.	Silicon oxy-nitride gate dielectric.
5.	Boron back-side gettering.
6.	Solid (Boron+) Boron diffusion source.
7.	Aluminum second-layer mask for channel stop implant.
8.	Additional oxidized polysilicon gate dielectric layer.
9.	Dry (plasma) etching of polysilicon.
10.	Processing using a model maker.
11.	Polysilicon/diffusion contact rework.

Since extremely uniform wafer thickness was not required on the current program, and since it was believed that particles of powdered silicon which were transferred to tne front of the wafers could cause defective lines, the

wafer back-grinding process was discontinued at the start of this program. However, subsequent analysis of the number of line defects on the back-ground lots processed immediately prior to this program (9.3 line defects per wafer, average) and the first lots processed during this program (9.7 line defects per wafer, average) indicated that grinding the backs of the wafers had no statistically significant effect on wafer yield.

Increased Gate Oxide Thickness

One lot was processed with the gate oxide thickness increased to 2000 A from the normal 1400 A in an attempt to determine if pinholes in the gate oxide were a significant cause of line defects. The experiment had exactly the opposite of the desired result; the number of defects per wafer was double that of a second lot run at almost the same time with the conventional gate oxide (13 defects per wafer compared to 5 defects per wafer). The increase in defects is probably due to some other unintentional variation in the process. The use of thicker gate oxide was not pursued, however, since it results in undesired increases in the transistor thresholds.

Increased Field Oxide Thickness

A permanent process change was made at the start of this program which increased the field oxide thickness to 6000 A from the 4000 A used on the predecessor program. It was expected that the increased thickness would reduce the number of line defects. However, an analysis of line yield on comparable lots indicated a reduction in average number of defects per wafer from 10.2 to 9.8. This change is well within normal process variations and does not indicate a strong dependence of defects on field oxide thickness.

Oxy-Nitride Gate Dielectric

Several devices from one lot received a gate dielectric composed of 800 A of thermal oxide followed by a 900 A layer of silicon nitride. These devices were then combined with the balance of the lot, which had received the normal 1400 A of thermal oxide. A comparison of the two gate dielectric structures is shown in Figure 8. Pinhole tests, performed after deposition of the gate dielectrics, showed about 25 pinholes per square inch for the oxide dielectric and only one pinhole per square inch for the two-layer insulator. After completion of the processing through the polysilicon level, tests for line defects indicated that the multi-level dielectric reduced the number of defects from 9.4 per wafer to less than 2 per wafer.

The results of the oxy-nitride gate dielectric experiment are significant. They demonstrate that pinholes in the gate oxide are a significant cause of line defects, and that a multi-layer dielectric can reduce the number of defects. However, the two-layer dielectric used in this experiment cannot be used in the fabrication of matrix circuits due to charge trapping on the oxide/nitride interface, which causes variations in the transistor thresholds. The charge trapping effect can be avoided through the use of a graded film, such as those recently developed for VHSIC circuits using thermal nitridation of oxide films in ammonia gas at high temperatures

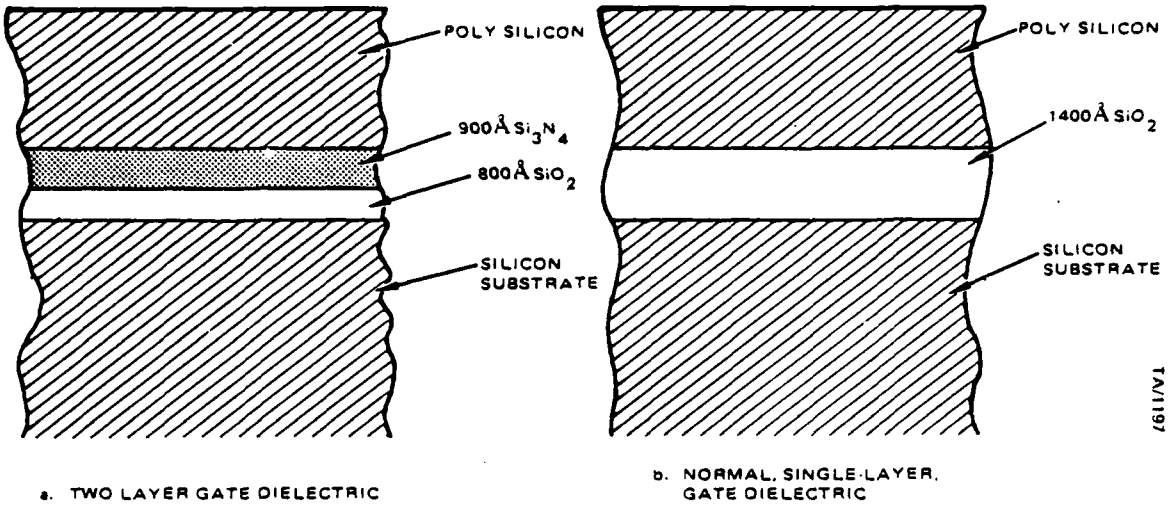


Figure 8. Alternative gate dielectrics.

(see Ito, Nozaki, and Isikawa, J. Electro. Soc. 127, p. 205, and Koong, Van Licrop, and Appels, J. Electro. Soc. 123, p. 1117). This area has been identified for additional development after the conclusion of the current program.

Boron Gettering/Solid Diffusion Source

Under some circumstances, a heavy diffusion into the backside of a wafer, prior to any front-side processing, will attract and trap, or getter, impurities and dislocations from the front of the wafer. An experimental lot was processed to determine if back-side gettering could be used to reduce the number of defects in the matrix circuits. This experiment was combined with a second experiment to evaluate the use of a solid, as opposed to gaseous, boron diffusion source. The procedure used was as follows:

1. The front sides of all wafers were coated with sputtered silicon dioxide.

2. Boron from a Boron-Bromide source was diffused into the back sides of half of the wafers to a sheet resistivity of 12 ohms per square. The diffusion was then driven to a depth of 2 microns and a sheet resistivity of 20 ohms per square.

3. The silicon dioxide on the front sides of all wafers was patterned with the source/drain mask for the display matrix circuit. The wafers were divided into two groups, with each group containing wafers with and without back-side gettering. Boron was diffused into the source/drain regions of one group from a gaseous Boron-Bromide source; the second group received a diffusion from a solid Boron-Plus source.

4. Contacts were etched in the oxide (formed during the diffusion drive) over the diffused regions and doped polysilicon was deposited. The polysilicon was patterned into testable lines such that each wafer had 175 lines, each of which connected 175 diffused regions.

5. The wafers was electrically tested for shorts between the polysilicon lines and the substrate. The results of the tests are summarized in Table 3.

The results of these experiments were that, while the standard process produced the highest yields, the lowest yields were produced by the most novel process. These initial results are probably more indicative of the difficulty in initiating a radical process change than of any fundamental yield differences between the processes. Subsequent experiments, performed outside of the effort on this contract on a different display matrix circuit, indicate that the two diffusion processes may be used interchangeably without any effect on yield.

TABLE 3.

GETTERING/DIFFUSION EXPERIMENT RESULTS

	% Yield of Unshorted Lines	
	Gettered	Not Gettered
BBr3 Diffusion Source:	95.9	99.8
Boron Plus Diffusion Source:	74	98.3

Aluminum Channel Stop Mask

The integrity of the masking during the channel stop implant has long been identified as having a major impact on the number of shorted drain lines on the matrix circuit. Numerous variations in the masking procedure for this implant have been studied. At the start of the current program, the standard masking procedure was as follows:

1. The layer of thermal silicon dioxide resulting from the combination of the initial oxide and the boron diffusion drive is patterned and etched using one copy of the channel stop mask.

2. A additional layer of photoresist is deposited and patterned using a second copy of the channel stop mask.

3. The two-layer photoresist/oxide structure is then used to mask the implant.

The major problems associated with this process were the extra handling of the wafers associated with the second masking step, and the difficulty in removing the photoresist mask layer after the implant. During this program, an alternative process, in which an aluminum layer is used instead of photoresist as the second mask layer, was developed and used on half of the wafer lots. This new process adds an additional step, the aluminum deposition, but has the advantage that the aluminum is easy to remove after the implant.

The results of these tests, as summarized in Table 4, show that the type of channel stop mask does not effect the total number of defects. Both masking procedures produced an average of 9.8 defects per wafer.

TABLE 4.

ALUMINUM CHANNEL STOP MASK RESULTS

		Average Number of Line Defects Per Wafer							
		Photoresist Mask				Aluminum Mask			
Lot #	# of Wafers	DO	DS	GO	GS	DO	DS	GO	GS
50	10	1.1	2.6	0.4	6.1				
51	5					0.6	3.8	0.8	2.8
52	6	4.1	3.1	0	3.5				
53	7					0.6	7.0	0	0
55	11					2.6	2.9	0	6.5
56	10	0	0.3	1.8	6.9				
Averages		1.4	1.8	0.8	5.8	1.6	4.3	0.2	3.7

The results of these experiments did show that the masking procedure influences the type of defects. The use of the aluminum mask reduces the number of gate shorts, but increases the number of drain shorts. The reduction in the number of gate defects is not totally unexpected; the wafers processed using aluminum are cleaner after implant and thus they incur fewer oxide defects during later processing. The increase in the number of drain shorts is not yet well understood.

Oxidized Polysilicon Gate Dielectric

A previous process experiment had demonstrated that the number of line defects could be reduced through the use of a two layer oxide/nitride gate dielectric. This gate dielectric structure could not be used in actual

devices because of charge trapping at the oxide/nitride interface. A second experiment was performed to determine if a two-layer oxide dielectric, where the two layers are deposited by different processes, would provide a similar reduction in line defects. The detailed procedure was as follows:

1. A lot of wafers was processed through the normal gate oxide growth.

2. 500-600 A of undoped polysilicon was deposited on eight of the wafers and oxidized completely.

3. All wafers were completed with the normal contact etch and polysilicon deposition and patterning.

After completion, the wafers were tested for shorts between the polysilicon lines and the substrate. The wafers with the two-level gate insulator had an average of 5 shorts per wafer, while the normally-processed wafers had an average of 34 shorts per wafer. Because of this distinct improvement, the two-level gate dielectric process was implemented on half of the wafers from four subsequent lots. Unfortunately, these subsequent lots had bad polysilicon/diffusion contacts on those wafers which received the two-level gate structure and additional test data on the two-level gate structure could not be obtained.

Several process variations were tried to determine the cause of the bad contacts. The problem was traced to a faulty furnace which allowed oxide growth in the contacts prior to the deposition of the polysilicon gate layer. Two such furnaces were available to deposit the gate material. The wafers with the two-level gate dielectric were all processed in the faulty unit, while the conventional wafers were processed correctly.

Plasma Polysilicon Etching

At the start of the current program, the standard process for patterning the polysilicon layer was a wet chemical etch. Dry plasma etching was used on several lots during the program without any significant effect on device yield.

Aluminum-Silicon Gate

The majority of the matrix circuits constructed on this program were processed with polysilicon gate electrodes. This process was originally selected because of the excellent step coverage of Low Pressure Chemical Vapor Deposited (LPCVD) polysilicon. Additionally, this material allows the subsequent use of silicon dioxide deposited at high temperatures as the interlevel insulator.

One half of the wafers in one lot were processed using aluminum/silicon as the gate electrodes. The potential advantage of this material is that its low resistivity, compared to polysilicon, allows the use of a thinner layer,

thus decreasing the height of the contours which must be covered prior to depositing the mirror electrodes. A direct comparison between the two halves of this lot could not be made because the wafers with the conventional gate material had bad polysilicon/diffusion contacts. The wafers with the aluminum/silicon gates had yields similar to those of other lots processed separately.

Model Maker Processing

The fabrication of the initial lots of wafers on this program was accomplished in a conventional manner with each process step performed by a different person. On later lots, a single experienced process technician (the "model maker") performed all process steps. This change was expected to reduce the number of defects because the model maker was intimately familiar with the stringent handling and masking requires of the large matrix circuits.

A transition to model maker processing was also made on a different display matrix circuit being fabricated on a separate effort. The results on the two matrix circuits were similar; the average device fabricated by either model maker had 30% fewer defects than the average device fabricated conventionally.

Polysilicon/Diffusion Contact Rework

A number of wafers processed during this program were found to have bad contacts between the polysilicon level and the underlying diffusions. Some of these wafer were reworked by replacing the polysilicon level with aluminum. Other wafers were repaired with a new process developed on this program. The same contact problem also occurred on one lot of wafers processed on the predecessor program. Many of those wafers were used to develop the rework processes. The new process developed to repair the contacts is shown schematically in Figure 9. The steps in this process are performed as follows:

1. The wafer is coated with photoresist and exposed using the contact mask.

2. A one-micron layer of aluminum is deposited on the wafer.

3. The photoresist is removed, leaving aluminum over only the areas above the polysilicon/diffusion contacts.

4. The wafer is cleaned and annealed at 450 C in forming gas (Nitrogen + Hydrogen) for 45 minutes. This step diffuses the aluminum preferentially through the polysilicon and through the underlying thin oxide layer. The aluminum "spikes" which penetrate the oxide establish the needed electrical contact.

5. The excess aluminum is then removed from the top of the wafer, and the device is finished using only low temperature process (to

avoid diffusing the aluminum through the diffusion into the substrate).

This novel process has been highly successful in correcting the bad contacts. Of the 28 wafers processed in this manner, 22 had normal drain line resistance and a normal number of defects. The six wafers that were processed unsuccessfully were all from one lot and apparently had a thicker layer of oxide between the polysilicon and the diffusions.

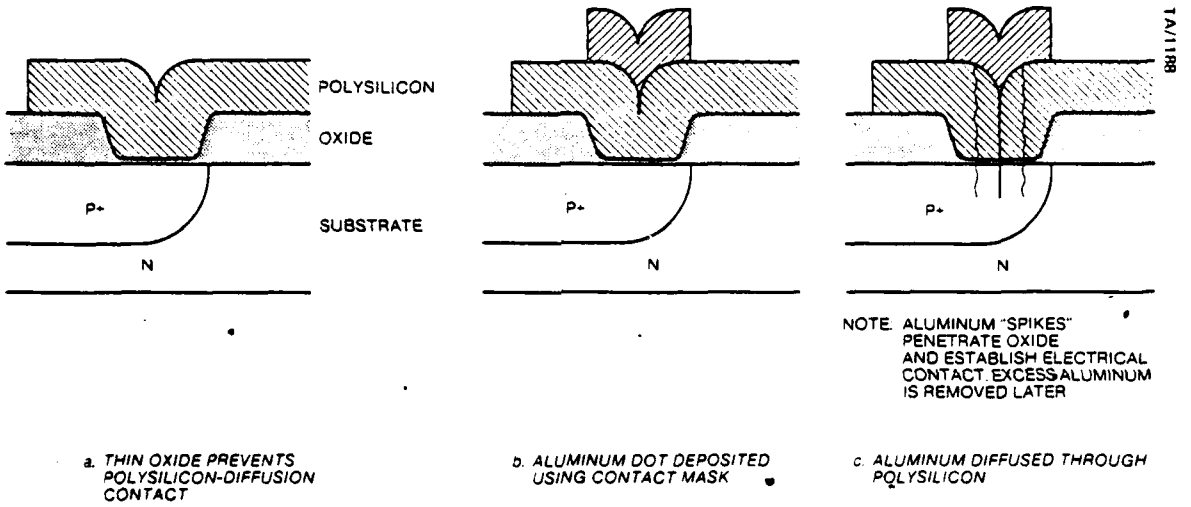


Figure 9. Polysilicon/diffusion contact rework process.

The earlier method of repair, replacing the polysilicon layer with aluminum, was less successful. Only 14 of the 27 wafers attempted had normal drain line resistances and a normal number of drain line opens. These poor results were traced to the poor step coverage of the 2000-3000 A layer of aluminum. A thicker aluminum layer could not be used because of the requirements of later process steps.

3. WAFER TEST

After the patterning of the polysilicon layer, the wafers are subjected to an exhaustive series of electrical tests. During the course of this program, several significant modifications were made to the test procedure. Tests for shorts between adjacent pairs of gate or drain lines, and between gate lines and diffusions were added. The test reporting software was modified to provide a summary report for each wafer which identifies (by number) defective lines and which distinguishes between gate/substrate and

gate/diffusion shorts. Additionally, a database for storing the test results on disc was established to allow future analysis of the yield data. At the conclusion of this program, the standard test procedure consisted of the following sequence of tests:

a. Transistor Function Tests

Transistor function tests are performed on test devices located outside of the perimeter of the display matrix. The parameters that are measured include gate threshold voltage, diffusion breakdown voltage, and punch-through voltage. Diffusion breakdown voltage is defined as the voltage between any source or drain diffusion and the substrate which causes a current flow of 10 micro-amps. Punch-through voltage is defined as the voltage between the source and drain of a transistor which cause a current flow of 10 micro-amps with the gate at substrate potential. Typical values for these parameters are a threshold voltage of -2 volts, and breakdown and punch-through voltages of -50 volts.

b. Drain Line Yield

Three tests are performed, using computer controlled instruments and an automatic probe system which steps from line to line, on each drain line of the display. A photograph of the test system is shown in Figure 10. The first test is the measurement of the resistance between the two ends of the line, typically 100K ohms. Any line with a resistance above one megohm is defined as open. For the second test, both ends of the line are placed at -30 volts with respect to the wafer substrate, and the current flow between the line and the substrate is measured. A current flow above 75 micro-amps is defined as a short. Lines with leakage currents above this value may not function properly in a completed display, while lines with lower leakage currents generally do not cause a visible display defect. The final test is a measurement of leakage current between adjacent pairs of drain lines. The typical value for this leakage is less than one micro-amp, and shorts between adjacent lines are very rare. This series of tests is performed at a rate of approximately one line every two seconds.

c. Gate Line Yield

After completion of the drain line tests, the wafer is rotated 90 degrees, and the same automatic probes are used to perform a series of four tests on each gate line. The same probe assembly can be used since the wafer is symmetric. The same three tests that were performed on each drain line are performed on each gate line. In addition, +3 volts (with respect to the substrate) is applied to the ends of the gate lines and the current flow to the substrate is measured. An appreciable current will flow in any gate line that is shorted to a source or drain diffusion. This type of short is not

Figure 10. Automated wafer test equipment.

detected by the previous tests, since the junction between a diffusion and the substrate does not conduct when a negative voltage is applied.

After the series of tests is completed, the computer prints a summary of the test results for each wafer. A typical recent test summary for a wafer at the polysilicon test is shown in Figure 11. This data has been retyped from the original for clarity.

At the top of the test summary shown in Figure 11 is a listing of the defective line numbers. In this example, drains lines 109 and 140 are open (DO). Note that open drain line number 109 is indicated by a line resistance value of 0.00. Similarly, the line numbers are listed for drains shorts (DS), gates opens (GO), and gate shorts (GS). Following this information is a header which identifies the wafer under test (lot 56, wafer 16), the stage in the process at which the tests were performed (polysilicon with aluminum spike

DO 109 140 GO 46
DS 167 170 GS 1 96 111

IDENTIFICATION: MXL-56-16 AT POLY/AL

DATE: 12:15 PM FRI. 9 APR. 1982 97.7% YIELD

DOPEN- 2 DSHT- 2 GOPEN- 1 GSHT- 3

	DRAINS		GATES	
LINE	RESIS	CURNT	RESIS	CURNT
1	138.26	.03	47.88	658.43
2	146.17	.01	48.21	-.02
3	152.14	.01	49.14	-.00
4	174.13	.01	48.47	-.02
±	±	±	±	±
108	106.00	.03	62.44	-.01
109	0.00	.00	54.36	-.01
110	105.20	.00	63.30	-.02
111	109.56	.01	50.01	-502.50
112	103.71	.00	53.36	-.01
±	±	±	±	±
167	98.59	987.68	48.47	-.01
168	115.02	.02	48.85	-.01
169	99.53	.03	48.63	-.00
170	99.78	237.73	49.11	-.01
171	100.97	.00	47.85	-.02
172	101.03	.02	47.82	-.02
173	100.74	.00	51.39	-.02
174	101.21	.00	49.58	-.02
175	102.13	.00	48.81	-.01

Figure 11. Typical wafer test summary.

rework), the date and time of the test (April 9, 1982, 12:15 PM), and the overall percentage yield of good lines (97.7%).

On the next line of the report is a summary of the quantity of bad lines (2 drain opens, 2 drain shorts, 1 gate opens, and 3 gate shorts). The lower section of the report is a listing of the test data. In Figure 11, the data has been selected such that several of the defective lines are shown. The line resistances are given in kilo-ohms, and the leakage currents are in micro-amps.

The printed gate leakage current value is the larger of the currents measured at -30 volts and at +3 volts. Thus the sign of the current distinguishes between gate/diffusion and gate/substrate shorts. Gate line 1 has a high positive current flow; this line is shorted to a diffusion. Gate

line 111 has a high negative current flow and is, therefore, shorted to the substrate directly.

4. WAFER PROCESSING RESULTS

The following tables list a summary of the line yield data for each wafer in the final seven lots processed on this program. Each table contains the data from one lot. The even numbered wafers in lots 50 thru 53 had, as previously described, bad contacts between the polysilicon and the diffusions. A similar problem occurred on half of the wafers in lot 56. Drain line yield data is given for these wafers only if they were reworked by one of the two processes previously described. Since the contact problem was caused by an improperly installed furnace and is not expected to recur, these wafers are listed as "not completed" in the summaries at the bottom of the tables unless successfully reworked. Note that wafer number 20 in each lot is removed early in the processing for quality assurance tests, and that the final lot had 21, instead of 19, wafers.

The combined results of these seven lots were that 32% of the wafers started were completed with ten or fewer defective lines. 29% of the wafers had more than ten defects, and 39% of the wafers started were not completed or had bad contacts.

TABLE 5.

LINE YIELD AT POLYSILICON TEST POINT

LOT 50

Wafer Number	Number of Defective Lines				
	DO	DS	GO	GS	Total
1	1	1	0	5	7
2	-	-	0	0	-
3	1	5	0	0	6
4	-	-	-	-	-
5	4	1	5	3	13
6	-	-	-	-	-
7	0	2	0	10	12
8	-	-	0	0	-
9	0	0	0	6	6
10	-	-	0	14	-
11	1	10	0	3	14
12	-	-	0	24	-
13	1	3	12	17	33
14	-	-	0	0	-
15	1	2	0	3	6
16	-	-	-	-	-
17	1	3	0	2	6
18	-	-	0	4	-
19	0	3	3	16	22
20					

Total Number of Defects	Number of Wafers
0	
1	
2	
3	
4	
5	
6	4
7	1
8	
9	
10	
10+	5
Not Completed	9

TABLE 6.

LINE YIELD AT POLYSILICON TEST POINT

LOT 51

Wafer Number	Number of Defective Lines				
	DO	DS	GO	GS	Total
1	1	15	5	64	85
2	-	-	0	1	-
3	0	1	0	1	2
4	-	-	1	0	-
5	0	3	0	1	5
6	-	-	-	-	-
7	0	2	0	3	5
8	-	-	0	0	-
9	3	0	3	0	6
10	-	-	1	3	-
11	1	2	1	2	6
12	-	-	0	2	-
13	0	3	0	19	22
14	-	-	0	1	-
15	0	2	0	0	2
16	-	-	0	1	-
17	0	9	0	7	16
18	-	-	-	-	-
19	1	5	0	135	136
20					

Total Number of Defects	Number of Wafers
0	
1	
2	2
3	
4	
5	2
6	2
7	
8	
9	
10	
10+	4
Not Completed	9

TABLE 7.

LINE YIELD AT POLYSILICON TEST POINT

LOT 52

Wafer Number	Number of Defective Lines DO	DS	GO	GS	Total	
1	3	4	0	3	10	
2	73	3	0	3	-	Spike Rework
3						
4	1	0	0	30	-	Al Rework
5	12	1	0	5	18	
6	154	14	0	2	-	Al Rework
7	1	9	0	11	21	
8						
9						
10						
11						
12	68	8	1	0	-	Al Rework
13						
14						
15	39	2	2	0	43	
16	1	0	0	5	6	Al Rework
17						
18	0	9	0	0	9	Spike Rework
19						
20						

Total Number of Defects	Number of Wafers
0	
1	
2	
3	
4	
5	
6	1
7	
8	
9	1
10	1
10+	3
Not Completed	13

TABLE 8.

LINE YIELD AT POLYSILICON TEST POINT

LOT 53

Wafer Number	Number of Defective Lines DO	DS	GO	GS	Total	
1	0	2	0	0	2	
2	10	0	1	0	12	Al Rework
3	3	1	0	0	4	
4	1	0	0	0	1	Spike Rework
5	0	3	0	0	3	
6	8	0	8	1	17	Al Rework
7	1	0	0	0	1	
8	2	6	0	5	12	Spike Rework
9	0	11	0	0	11	
10	-	-	-	-	-	
11	34	7	0	0	41	
12	0	125	1	5	-	Al Rework
13	0	6	0	1	7	
14	0	18	0	6	24	Spike Rework
15	0	2	0	0	2	
16	0	2	0	6	8	Spike Rework
17						
18	1	1	0	2	4	Spike Rework
19	0	47	0	0	47	
20						

Total Number of Defects	Number of Wafers
0	
1	2
2	2
3	1
4	2
5	
6	
7	1
8	1
9	
10	
10+	7
Not Completed	3

TABLE 9.

LINE YIELD AT POLYSILICON TEST POINT

LOT 54

Wafer Number	Number of Defective Lines				
	DO	DS	GO	GS	Total
1					
2					
3					
4					
5	10	3	0	13	26
6					
7	0	13	0	28	41
8					
9					
10					
11					
12	4	6	1	5	16
13	3	8	0	27	38
14	0	19	0	17	36
15					
16	2	32	0	18	52
17					
18					
19					
20					

Total Number of Defects	Number of Wafers
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	
10	
10+	6
Not Completed	13

TABLE 10.

LINE YIELD AT POLYSILICON TEST POINT

LOT 55

Wafer Number	Number of Defective Lines				
	DO	DS	GO	GS	Total
1	1	1	0	0	2
2					
3	3	3	0	0	6
4	2	5	0	3	10
5	2	6	2	0	10
6					
7	2	4	0	13	19
8					
9	1	37	0	11	49
10	1	48	0	25	73
11	1	11	0	16	28
12	1	4	0	11	16
13	1	0	0	3	4
14	1	0	0	14	15
15					
16					
17	3	6	0	14	23
18	1	23	0	14	38
19	1	0	0	0	1
20					

Total Number of Defects	Number of Wafers
0	
1	1
2	1
3	
4	1
5	
6	1
7	
8	
9	
10	2
10+	8
Not Completed	5

TABLE 11.

LINE YIELD AT POLYSILICON TEST POINT

LOT 56 - ODD WAFERS HAVE AL/SI GATES

Wafer Number	Number of Defective Lines DO	DS	GO	GS	Total	
1	2	18	0	1	21	
2	1	2	1	8	12	Spike Rework
3	1	11	0	2	14	
4	2	7	0	3	12	Spike Rework
5	2	0	0	0	2	
6	1	0	0	2	3	Spike Rework
7	5	28	0	0	33	
8	1	1	0	3	5	
9	1	4	0	0	5	
10	1	4	1	3	9	
11	2	3	0	0	5	
12						
13	1	2	0	0	3	
14	1	2	0	1	4	
15	1	9	0	0	10	
16	2	2	1	3	8	Spike Rework
17	2	1	0	0	3	
18	1	3	0	4	8	
19	1	6	0	0	7	
20	2	3	0	10	15	Spike Rework
21	0	1	0	0	1	

Total Number of Defects	Number of Wafers
0	
1	1
2	1
3	3
4	1
5	3
6	
7	1
8	2
9	1
10	1
10+	6
Not Completed	1

SECTION III.

DISPLAY ASSEMBLY

1. INTRODUCTION

The silicon matrix addressing circuits used in the 175x175-element liquid crystal display modules constructed on this program are fabricated and tested using the procedures described in section II. After completion of the electrical tests at the polysilicon level, an additional series of proprietary processes are used to deposit an array of optical-quality mirror electrodes which define the individual display picture elements. The electrical test described in Section II. are repeated after deposition of the mirror electrodes. The matrix circuits are then ready to be assembled into display devices.

The basic assembly procedures are illustrated schematically in Figure 12. The steps of the display assembly process are as follows:

a. The square matrix array is sawed from the circular wafers using a conventional Tempress wafer dicing saw. The excess silicon is discarded and the matrix circuit is cleaned to remove silicon particles and the saw lubricant.

b. The matrix circuit is mounted to a glass circuit plate. The circuit plate, as shown in Figure 13, has a gold metallization pattern which includes 175 lines which pass under the matrix circuit to provide redundant drive to the columns of the display. A mylar preform coated with a thermo-setting epoxy is placed between the back of the matrix circuit and the glass substrate. The top side of the matrix circuit is pressed onto a glass optical flat while the epoxy is cured.

c. A surface treatment is then performed on the matrix circuit to ensure proper alignment of the liquid crystal material. As will be described in the next section, a variety of surface treatments were used during the program.

d. A glass cover plate, coated with a transparent electrode and treated for liquid crystal alignment, is then mounted on top of the matrix circuit. An epoxy-coated mylar spacer is used between the circuit and the cover glass to form a sealed cell for the liquid crystal material. The thickness of the mylar spacer is controlled to maintain a constant 12.5 micron cell thickness. The mounted

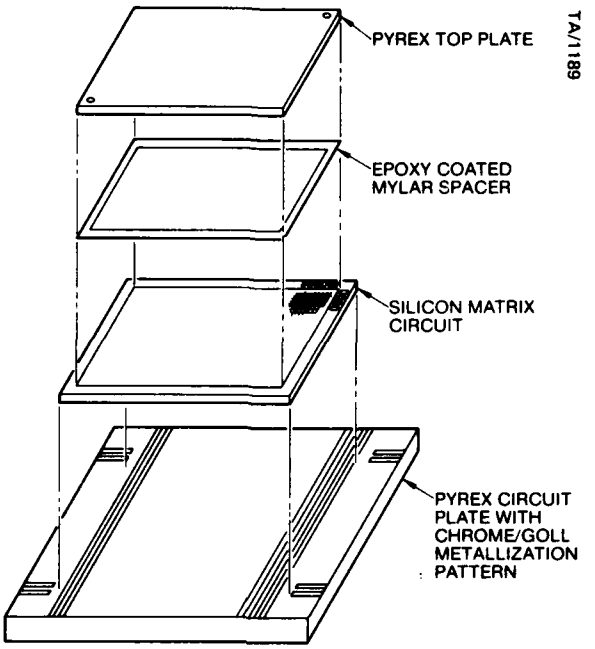


Figure 12. Display assembly process.

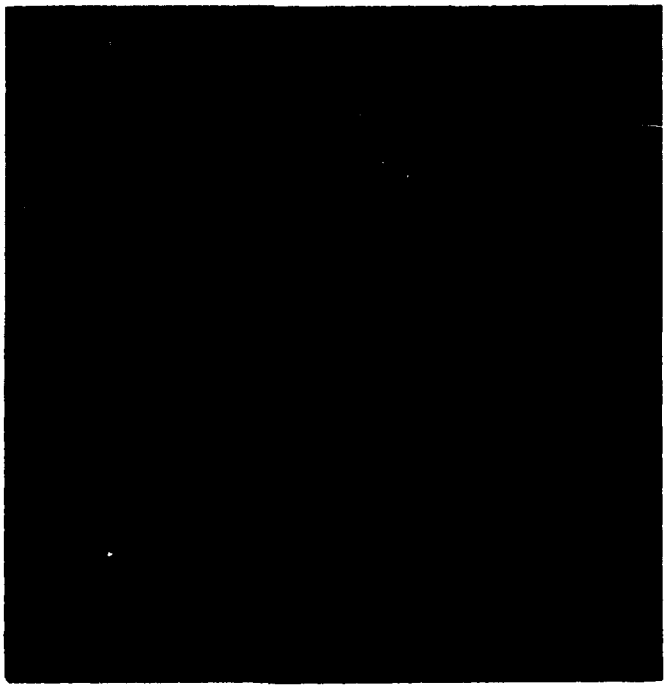


Figure 13. Glass substrate with gold circuit pattern.

matrix circuit, the spacer and the cover glass are clamped together and placed in an oven to cure the epoxy. After cure, the assembly is inspected for epoxy adherence, leaks, and excessive epoxy flow. Then a bead of a second epoxy is run around the outside of the spacer for additional mechanical strength.

e. The liquid crystal material is introduced into the assembled cell through two holes which were previously drilled in the extreme corners of the cover glass. An infusion syringe pump, inserted through a septum sealed over one hole, is used to push the liquid crystal material into the cell. After the cell is filled, the liquid crystal material is briefly activated and then the liquid crystal material is removed using a combination of nitrogen gas pressure and vacuum at the two fill holes. The cell is then refilled and indium plugs are inserted into the two fill holes.

f. The display is then tested for proper video operation on a special probe station. The top of the cell is then cleaned, and epoxy is applied to reinforce the indium plugs in the fill holes.

g. The final step in the display assembly is to install wirebonds between the matrix circuit and the glass circuit plate. Ultrasonic bonding with aluminum wire is used to avoid heating the display substrate. After bonding, the display is again tested for proper operation. Faulty wirebonds are repaired, and the bonds are coated with plastic for mechanical protection.

2. DISPLAY ASSEMBLY PROCESS DEVELOPMENT

A number of modifications were made to the assembly processes during this program. These developments are described in the following subsections.

Multi-layer Transparent Electrode

Proper operation of the liquid crystal display module in a projection system requires that the specular reflections from the module be minimized when the liquid crystal material is energized. These specular reflections arise front the first surface of the cover glass, and from the transparent electrode within the cell. The reflections from the first surface can be directed away from the projection optics and are not of major concern. However, the reflections from the transparent electrode cannot be removed through optical techniques and must be minimized.

Prior to the start of this program, the liquid crystal display modules were constructed using a single layer indium-tin oxide transparent electrode. This coating has a high index of refraction, compared to the liquid crystal material and the cover glass. The specular reflection from this coating is low only at the wavelength which is twice the optical thickness of the coating, and increases as the wavelength is changed from this value. Thus the display contrast is maximized at one wavelength, as shown in Figure 14.

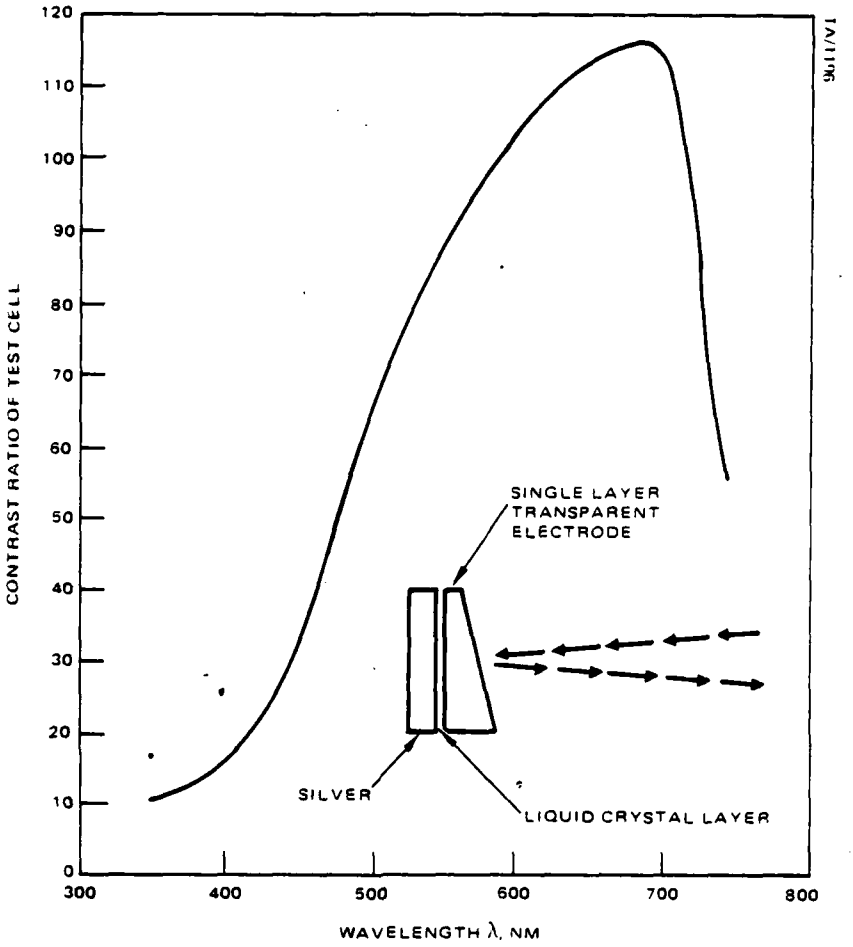


Figure 14. Display contrast varies with wavelength for single-layer transparent electrode.

Figure 14 shows that high display contrast can be obtained only if the optical thickness of the transparent electrode is precisely matched to the wavelength of operation. The optical thickness of the coating is dependent on both the physical thickness and the index of refraction. Although several vendors were used to coat the display cover glasses, consistent control of the coating optical properties could not be achieved.

To avoid the problems associated with a single-layer transparent electrode, a change was made to a multiple layer coating. This coating was designed by a vendor for use in a similar application and has a reflectivity of less than one percent for wavelengths between 425 and 700 nanometers. Thus minor variations in the coating or changes in the wavelength of operation do not degrade the display contrast.

Alignment Surface Treatment

Maximum display contrast and video response times can be obtained only if the liquid crystal material assumes a regular molecular alignment when unenergized. The required alignment is obtained by proper treatment of the display surfaces which are in intimate contact with the liquid crystal material. This treatment causes one particular orientation of the liquid crystal molecules to have minimum potential energy, and thus creates a restoring force which forces the desired alignment.

The alignment surface treatment used on the matrix displays constructed on previous programs was to etch the surfaces using an ion beam. This technique is capable of producing good alignment, but is not consistent. After several alignment failures had occurred in otherwise good displays, alternative alignment techniques were investigated.

A well known alignment technique used in commercial display devices is the deposition of silicon dioxide at oblique angles. Several displays were constructed using this technique. Consistent alignment was obtained, but several of the displays had an unusual residual image storage that appeared to be caused by charge trapped on the nonconductive oxide. This effect does not occur in commercial displays using field effect liquid crystal materials which are also nonconductive, but apparently does occur in the matrix displays using a conductive dynamic scattering liquid crystal material with DC drive voltages.

A second alignment approach used in commercial liquid crystal displays is to rub the surfaces in one direction with a soft cloth. The approach was also attempted, but resulted in unacceptable scratches on the soft silver mirror electrodes.

A modified rubbing technique was developed and used in most of the display devices constructed on this program. A thin (about 200 A) polymer layer is spun onto the mounted matrix circuit and baked. After baking, the polymer surface is buffed in one direction with a cloth to create fine grooves in the polymer. The polymer coating prevents scratching the silver mirror electrodes. The cover glass is buffed in a similar manner, but without the polymer coating. This technique was used to produce display devices with good alignment, fast response, and little, if any, image storage.

Increased Cover Glass Size

The display matrix circuit is fabricated on a 3-inch silicon wafer. Thus the maximum outside dimension of the circuit is 2.05 inches square, and only 0.15 inch is available on each side of the active display area for the seal and wirebonds. These constraints lead to an original design in which the two fill holes were located well within the active display area where they obscured part of the displayed information. The majority of the perimeter around the active area was reserved so that the operator of the wire-bonder could observe the bonding operation over the edge of the cover glass.

An improved procedure, in which the operator views the bonding operation from the side, was established during the development, outside of this contract, of a smaller display device. Once perfected, the procedure was also used on the display devices constructed during the latter portion of this program. Since less room is reserved for the bonding operation with the new procedure, the size of the cover glass was enlarged, and the fill holes were moved to the very edge of the active area.

Pump Fill Procedure

Over the course of the development of the liquid crystal matrix displays, a number of cell filling techniques have been tried. Most of these techniques were only partially successful and commonly resulted in displays with nonuniform performance.

Two basic types of nonuniformities can occur in the matrix liquid crystal display devices. The first type is dark streaks, or filling marks, visible when the display is not energized, caused by localized areas with nonuniform liquid crystal alignment. These marks appear where ever the leading edge of the liquid crystal material is stopped during the filling operation; they do not appear if the material is introduced into the cell with a smooth continuous flow. The exact physical mechanism which produces these marks is not understood. Once the marks appear in a cell, they can be only partially erased by removing all of the liquid crystal material from the cell and refilling.

The second type of nonuniformity which appears in the matrix displays devices is a gradual variation in the amount of scattering in the liquid crystal material. The most common form of this effect is a continuous decrease in the scattering intensity across the cell, with the greatest intensity at the fill hole where the liquid crystal material is introduced, and the lowest intensity around the opposing fill hole. The cause of this type of nonuniformity is absorption of the conductive dopants in the liquid crystal material onto the display electrode surfaces. The liquid crystal material farthest from the fill hole traverses more surface area before reaching its destination and loses more dopant than the material adjacent to the fill hole. The solution to this problem is to fill the display cell several times until an equilibrium condition has been reached and further adsorption of the dopants does not occur.

The display filling procedure developed during this program and described in the introduction to this section uses the apparatus shown in Figure 15. The liquid crystal material is injected into the display through a septum using a syringe pump. This technique assures a controlled uniform flow of material across the cell and avoids filling marks. The display is filled two, or occasionally three, times. The first load of liquid crystal material is allowed to rest in the cell to coat the electrodes with dopant; the second filling then results in uniform display performance. Two fill holes, located in diagonally opposed corners of the cell, are provided to ensure that the display can be completely emptied and refilled.

Figure 15. Display filling apparatus.

Operational Test Prior to Assembly

During previous programs and during the earliest portion of this program, a functional test of the matrix circuit was performed prior to the start of the display assembly procedure. The display matrix circuit was held in a vacuum chuck on a probe station and coated with liquid crystal material. A mylar spacer (without epoxy) and a cover glass were placed on top of the matrix circuit. A operational test of the completed "display" was then performed. The purpose of this operational test was to determine the number of line defects (to confirm the results of previous electrical tests) and point defects (which are not detected during the wafer probe tests) in the matrix circuit. After this operational test, the matrix circuit was cleaned and the assembly procedures described in this section were performed.

A recurring problem during the predecessor programs was discoloration of the silver mirror electrodes during the cure of the epoxy used to mount the matrix circuit to the glass substrate. This problem occurred most commonly

when the display circuit had been in storage for an extended period (i.e. several weeks) prior to display assembly. Several variations in storage conditions and the epoxy cure cycle were tried without success.

At the beginning of this program, surface analysis was performed on several of the discolored matrix circuits. Although this analysis did not determine the precise composition of the stains, it did indicate that the stains contained organic structures that could not be explained by exposure to atmosphere. The results of the surface analysis lead to the conclusion that the stains were caused, at least in part, by residual material from the operational test. Attempts to devise a better cleaning procedure to remove all of the liquid crystal material without damaging the silver mirror electrodes were unsuccessful.

The operational test prior to display assembly was then discontinued. This test had primarily served to detect shorts between gate and drain lines, which are now detected by a new gate/diffusion electrical test previously described, and defective elements. With the exception of a brief period during the development of a new mirror electrode deposition procedure, the display devices constructed on this program had few defective elements. Thus little was lost by discontinuing the operational test, and the electrode staining problem was resolved.

Alternative Mirror Electrodes

Because of the previously described problem with staining of the silver mirror electrodes, several test cells were assembled in an attempt to find an alternative, stain-resistant, mirror material. Two cells were constructed with gold mirrors (although gold is yellow in appearance, the reflectivity of gold at 546 nanometers is nearly as high as that of silver). Both of these cells failed immediately after assembly. In both cases, the failure mode was flaking of the electrode material. A third cell was constructed with aluminum mirrors. The liquid crystal material in this cell developed many bubbles after a few hours of operation. Previously constructed cells with aluminum mirrors also developed bubbles, indicating a chemical reaction between the liquid crystal material and the aluminum. A fourth cell was constructed with aluminum mirrors overcoated with transparent indium/tin-oxide (ITO). This cell also failed, but much slower that the cell with uncoated aluminum.

3. DISPLAY ASSEMBLY RESULTS

A total of six test cells and 44 functional matrix display were constructed on this program. Of the functional displays, 21 were completed without any problems during the assembly procedures. The assembly results are summarized in Table 12. A complete listing of the displays assembled is given in Table 13.

TABLE 12.

SUMMARY OF DISPLAY ASSEMBLY YIELD

Assembly Step	Symptom	# Displays (out of 44)	Step Yield
Mount Matrix Circuit to Substrate		0	100%
Alignment Treatment	Marks	3	93%
Assemble Cover Glass	Particles	3	82%
	Seal leaks	3	
	Seal in Active Area	2	
Fill Cell	Bubbles	2	80%
	Resistivity High	4	
	Contamination	1	
	Nonuniform Scatter	2	
Plug Fill Holes	Ball Shorts	2	95%
CUMULATIVE ASSEMBLY YIELD			55%

TABLE 13.

DISPLAY ASSEMBLY RESULTS

Date Code	Wafer Lot	Wafer #	Assembly Notes
80271	33	2	Ball Short
80301			Bubbles
80302	40	17	OK
80303	40	5	Particles, Alignment Spin Marks
80311	46	7	OK
80312	24	12	Bubbles, Aluminum Mirrors
80322	39	17	Alignment Coverage Poor
80343	26	7	OK Aluminum/ITO Mirrors

TABLE 13.

DISPLAY ASSEMBLY RESULTS (CONTINUED)

Date Code	Wafer Lot	Wafer #	Assembly Notes
80344			ITO Reflectivity Test Cell
80351			ITO Reflectivity Test Cell
80352	45	1	OK
80391	42	2	Particles
80392	42	1	OK
80393	40	14	OK
80411	42	9	Seal Leaks
80412	42	15	Seal Leaks
80462	42	7	Particles
80492	45	13	OK
81031	37	8	LX Resistivity High
81032	37	14	LX Resistivity High
81042	45	5	OK
81043	40	13	Ball Short
81111			OK
81112	42	18	Seal Leaks
81151	40	11	Bubbles
81152	43	18	LX Resistivity High
81161			Alignment Marks
81171	45	9	Contamination, Seal In Active Area
81172	43	9	OK
81223			Seal In Active Area

TABLE 13.

DISPLAY ASSEMBLY RESULTS (CONTINUED)

Date Code	Wafer Lot	Wafer #	Assembly Notes
81231	53	7	OK
81232			OK
81251			OK
81252			LX Resistivity High
81291			OK
81292	51	7	OK
81293	51	9	OK
81352	56	19	Nonuniform Scattering
81381	56	5	OK
81382	56	9	OK
81401			OK
81451			Contamination, Gold Mirror Test Cell
81452			Contamination, Particles, Gold Mirror Test Cell
82271	56	8	OK
82272	56	14	OK
82411	53	16	Nonuniform, Later Refilled
83121	52	18	OK
83122	53	4	OK
83123	53	18	OK
83131	55	7	OK

4. DISPLAY EVALUATION

After each liquid crystal display device was completed, a series of tests were performed to evaluate the display's optical and electrical performance. A minimum of three basic performance measurements were taken: reflectivity of the display surface, contrast between the on and off states, and speed of response during transitions between states. Additionally, the number of inoperative lines or point defects was recorded.

All of the display measurements were performed on one of three optical bench test fixtures. Figure 16 shows schematic diagrams of the two test stations used to measure the performance of the displays in a simulated projection optical system. Additional measurements of the scattering properties of some displays were made using the equipment shown in Figure 17.

Reflectivity

As will be described in the next section of this report, optimum operation of a matrix liquid crystal display in a projection system requires that the light incident on unenergized picture elements be specularly reflected through a small aperture in the optical system. However, not all of the light incident on an unenergized element reflects in the right direction; some of the light reflects from the sloped edges of the mirror electrode. In addition, depending on the process used to deposit the mirror electrodes, some light may reflect from non-planar areas within the mirror caused by insufficient coverage of underlying circuit features.

The light reflected from non-planar areas and edges of one element interferes with light similarly reflected from other elements to form a "star" pattern. This pattern, shown in Figure 18, resembles an interference pattern from an array of square apertures. The effect of this pattern in an optical projection system is to cause the display reflectivity (and thus the projection system brightness) to vary with the size of the system aperture.

The set-up shown in Figure 16-a was used to determine the relationship between display reflectivity and aperture size. A helium-neon laser beam was reflected form the display surface and directed towards a a large collection lens. A wedge was index-matched to the LXD so as to eliminate the first-surface reflection off the pyrex cover glass. The lens focused the reflected light from the unenergized display into a photodetector. A variable aperture placed at the lens measured the overall reflectivity as a function of the collection angle.

Figure 19 shows the reflectivity versus collection angle for a first surface mirror and two different types of matrix display devices. The difference between the absolute reflectivity of the mirror and the display surfaces can be explained by the difference in the active mirror areas. Both displays have lower reflectivity due to the nonreflecting gaps between the elemental mirrors. The surface quality of the reflecting portion of each mirror element is shown in the slope of the reflection curve. The steeper the curve, the smoother the surface.

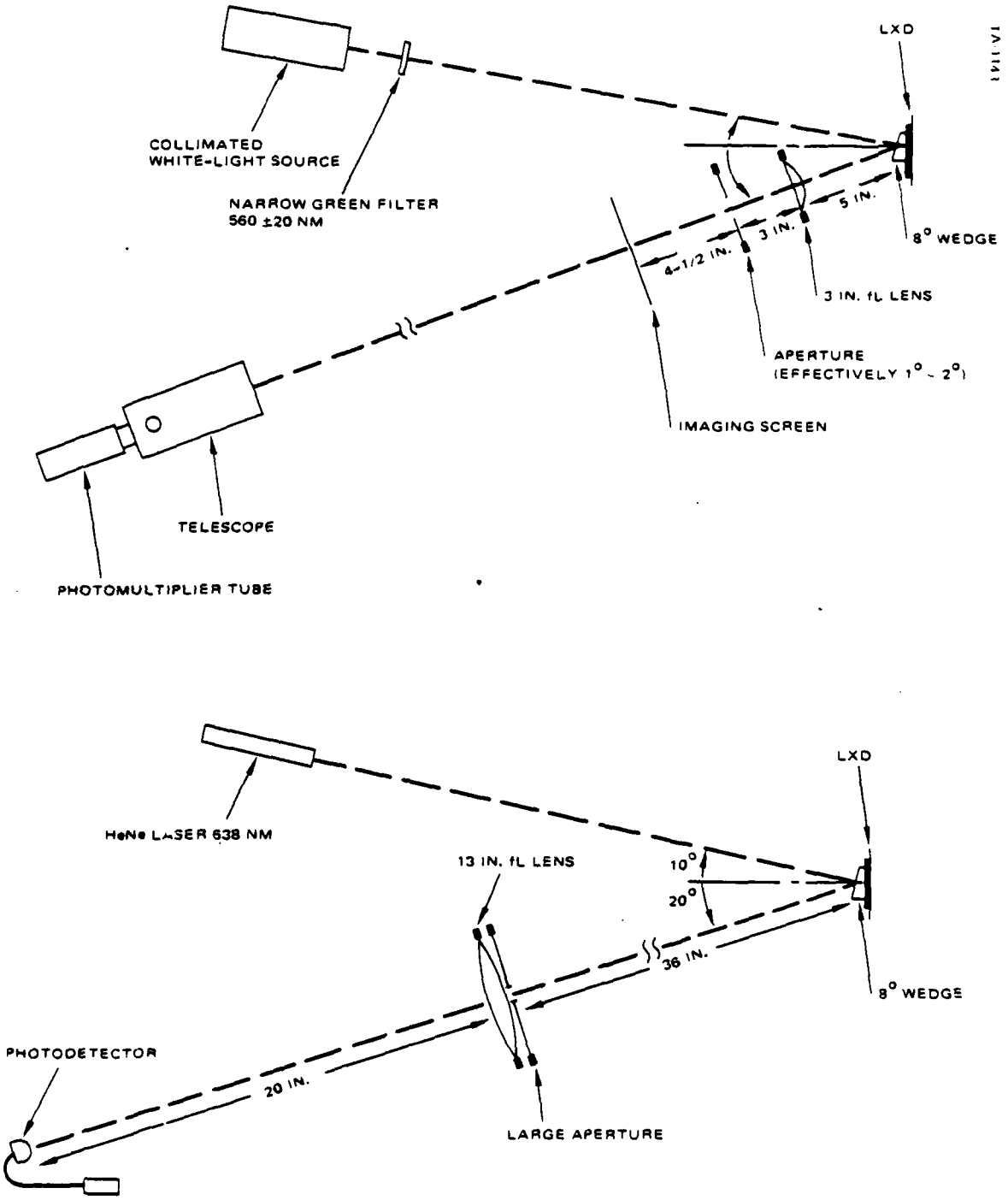


Figure 16. Test set-ups for measuring display performance in a simulated projection system.

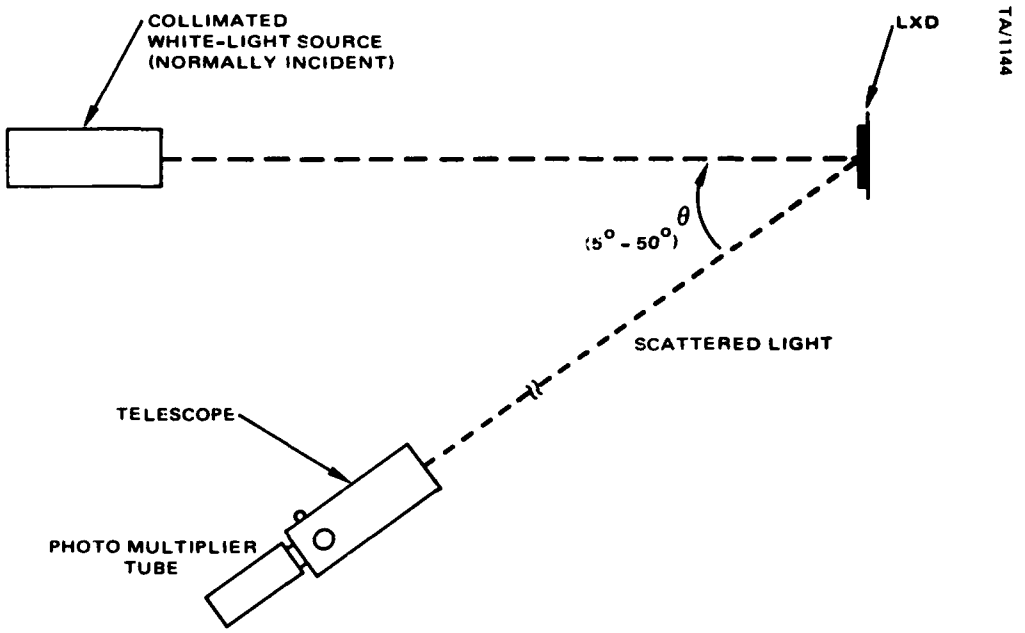


Figure 17. Test set-up for measuring display scattering.

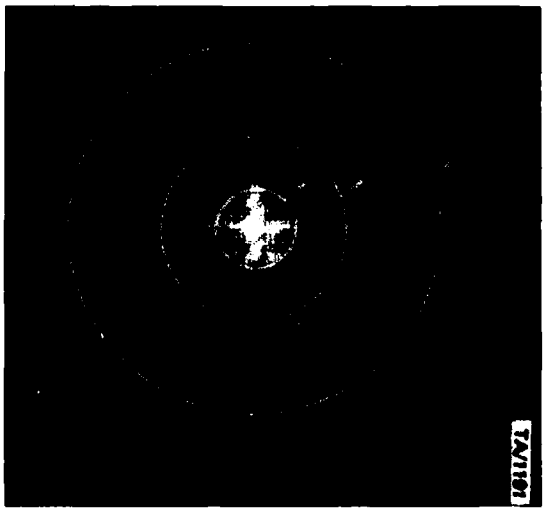


Figure 18. Reflection pattern from unenergized display.

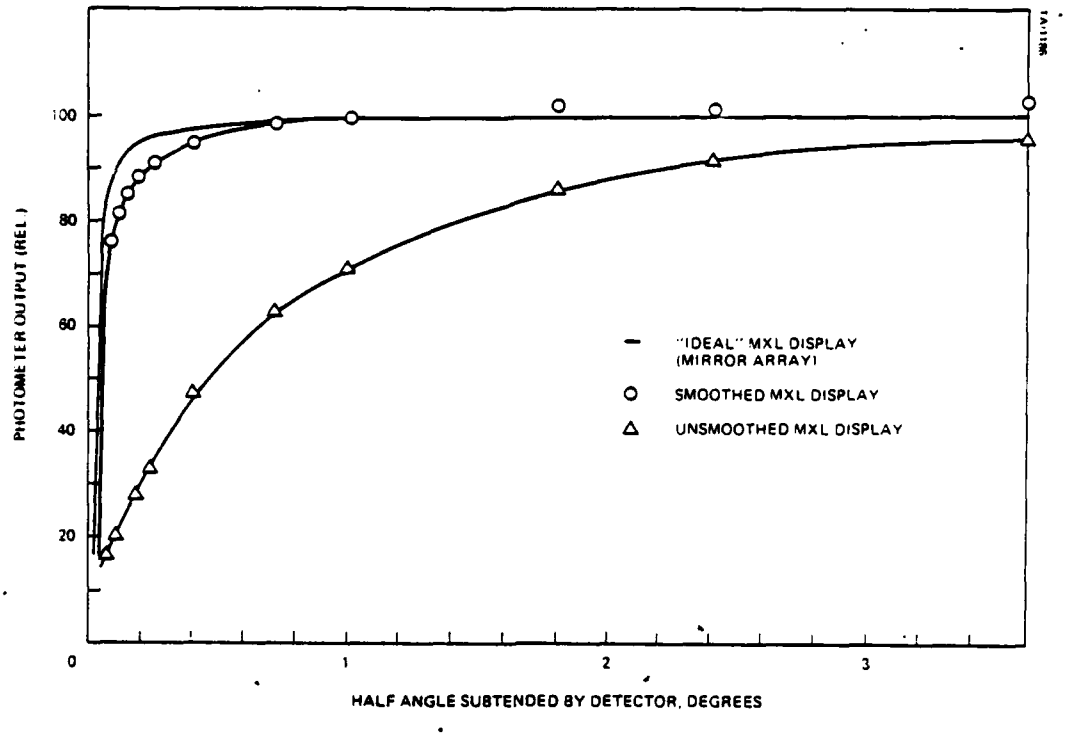


Figure 19. Reflectivity versus aperture size for a mirror and three different display devices.

In Figure 19, the "ideal" curve is data measured on a display in which the mirror electrodes were deposited directly on top of the matrix circuitry without any attempt to planarize the display surface. Thus the contours of the circuit structures are reproduced in the mirrors. The other two curves are data measured on displays where the circuit structures have been leveled by two different processes. The reflectivity of these displays is higher than that of the the non-planarized device for small collection angles.

Contrast Ratio

The absolute contrast of a matrix display is defined as the ratio of the reflectivities of the display (with a given collection angle) in the unenergized and energized states. As previously described, the reflectivity of an unenergized display varies with the collection angle, and with the process used to deposit the mirror electrodes. The reflectivity of the display in the energized state depends on the collection angle, the characteristics of the liquid crystal material and the transparent electrode in the display, and the RMS voltage across the liquid crystal layer. The RMS voltage across the liquid crystal layer varies with the peak voltage applied to the display, and, since the current required to energize the liquid crystal material is drawn from a capacitor at each element, the display refresh rate.

Additionally, the reflectivity of the transparent electrode varies as a function of the wavelength of the incident light.

The test fixture shown in Figure 16b was used to measure the contrast of the display devices. This fixture has provisions for varying the wavelength of the incident light and the collection angle. The electronics which drive the display have provisions to vary the peak voltage applied to the display columns and to provide either a DC level or a 30-200 Hertz pulse to the rows of the display. The following set of contrast measurements are made on each display tested:

a. Contrast versus the voltage applied to the columns of the display with a DC level applied to the rows, a fixed 2-degree collection angle, and green (550 nanometer) illumination.

b. Contrast versus collection angle with a DC level applied to the rows and columns of the display and green illumination.

c. Contrast versus refresh rate for a 2-degree collection angle, 550 nanometer illumination and DC applied to the columns of the display

d. Contrast versus illumination wavelength for a 2-degree collection angle and with DC applied to the rows and columns of the display.

Typical results of these contrast measurements are shown in Figure 20.

Scattering Measurements

To assist in locating display performance problems, the off-axis scattering properties of some displays were measured. Figure 17 shows the test set-up used to make these measurements. The intensity of the light scattered by the energized liquid crystal layer was measured as a function of angle and of the voltage applied to the columns of the display. No unexpected correlation was found between this data and the performance of the displays in a projection system. Thus these measurements served no unique purpose and were discontinued.

Speed of Response

The speed of response of the display was measured using either of the test fixtures shown in Figure 16. The rows of the display where set at a constant DC level and a 0-20 volt, one Hertz, square wave was applied to the columns. The analog output of the detector was displayed on an oscilloscope. Figure 21 shows the response of a typical display device. Both rise and fall times are defined as the period between 10% and 90% of the full-scale response. The difference in transition times is related to the relative ease in disrupting the aligned LX molecules but the difficulty in realigning these molecules. In a projection display, bright to dark (non-scattering to scattering) transitions are quicker than dark to bright.

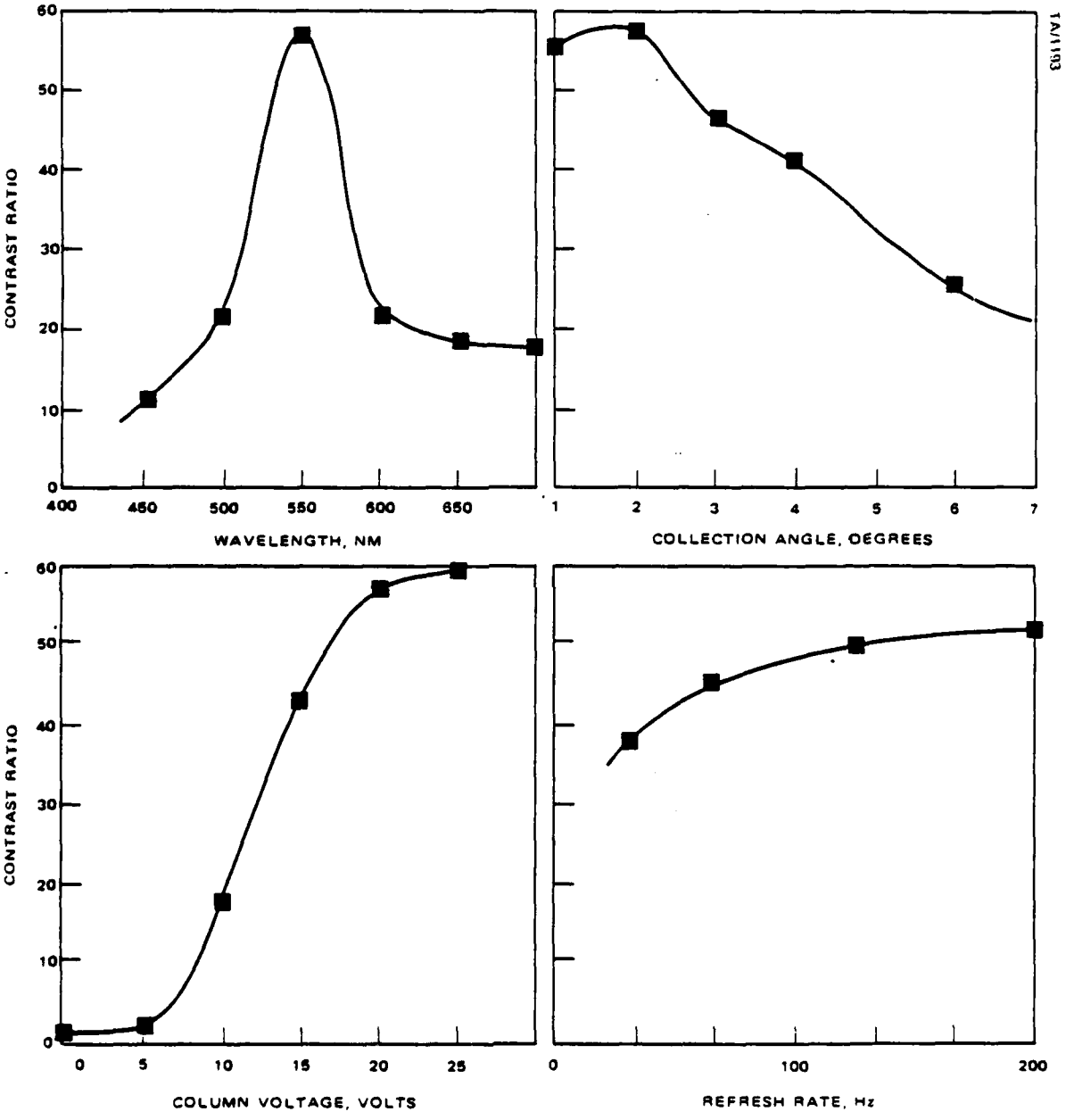


Figure 20. Results of contrast measurements on a typical display device.

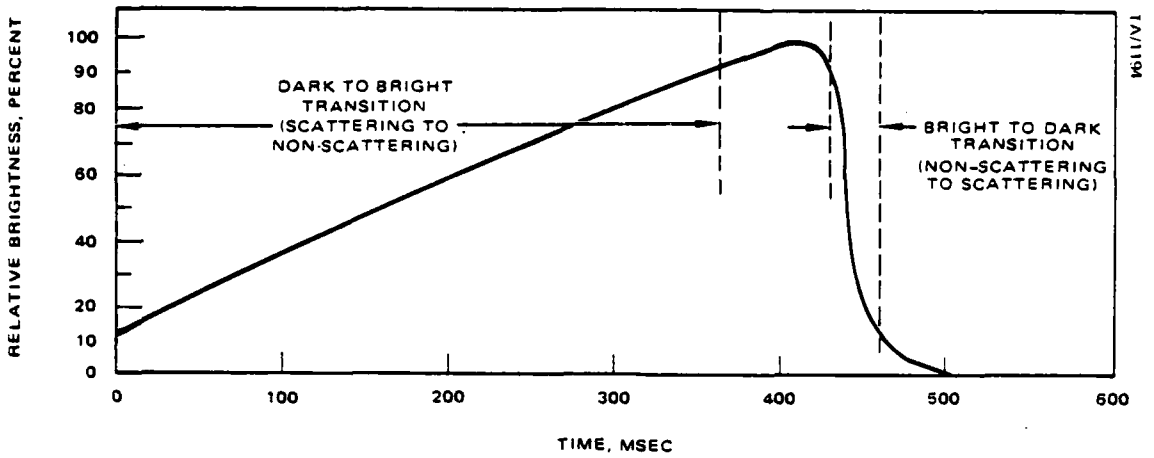


Figure 21. Typical display rise and fall times.

Blemishes

With the display fully scattering, a photograph of the display was taken to document the point defects, inoperative lines, and other nonuniformities in the LXD.

SECTION IV.

FOUR-MODULE PROJECTION DISPLAY DESIGN

1. BACKGROUND AND CONCEPT

The optical bench model of the four-module (Quad) projection display, previously shown in Figure 3, demonstrates the feasibility of optically aligning the projected images from four discrete liquid crystal modules to form a single continuous image. The design of the optical bench Quad was guided by the following overall areas of concern:

1. Appreciable distortion along the abutted edges of the four images would leave a noticeable gap between quadrants or would cause the loss of some information due to overlapping of images. Thus the prevention of geometric distortion along the edges of abutted images was one major consideration in the optical design.

2. The requirement for high brightness (in excess of 1000 foot-Lamberts) over a large viewing screen dictated the need for efficient light collection from the illumination source.

3. The need for gray shades for video display required sufficient contrast ratio between the "on" and "off" states of the LXD projector system. To provide maximum contrast, the design of the optical system had to be optimized to the performance of the liquid crystal modules.

4. Overall brightness uniformity had to be maintained across the entire image plane within a 2:1 difference (which the eye cannot detect over a large area). In addition, localized nonuniformities along the aligned edges of the four image quadrants had to be completely eliminated so as to produce the illusion of a single continuous display.

5. The overall design concept had to be consistent with future liquid crystal module formats and configurations, and with future high resolution display applications. Not only will different sizes of liquid crystal modules be combined (a 240x320-element display module with hybridized electronics has been developed), but more than four modules may be combined in some applications to further increase the resolution of the image.

6. The selected design for the optical bench Quad could not require lenses which call for unrealistic mechanical tolerances or shapes.

Two baseline approaches to a four-module projection display were conceived prior to the start of this program and described in the technical proposal for this effort. These alternative approaches are pictured in Figure 22. The approach shown in Figure 22a uses a single lens to simultaneously project the image the four liquid crystal modules. The advantages of such a system are (1) the use of a single lamp for a greater ratio of collected light to input power, (2) the inherently low distortion at the abutted edges of the four image quadrants (the design folds the virtual images of the four liquid crystal modules in such a way as to guarantee the absence of distortion along the aligned edges), (3) the small angular difference between the axial rays which decreases the amount of brightness discontinuity across the aligned edges, and (4) the overall compact arrangement of the entire package. The disadvantages of this approach are the mechanical complexity of mounting the components, and the large diameter of the single projection lens. Additionally, this approach cannot be directly extended for combining the images from more than four liquid crystal modules.

The second approach, shown in Figure 22b, uses a dedicated projection lens for each liquid crystal module. The major advantage of this approach is that it can be directly extended to display systems using six or more liquid crystal modules, each projected through its own lens. Additionally, the four-lens system has a simpler mechanical structure, and the speed of each projection lens group can be much slower than the single projection lens described in the first approach. However, each of the four projection lenses must be designed to produce an image with virtually no distortion. The major disadvantage to this system is the large angular difference between the edge rays of each quadrant which, if used with a conventional high gain screen, will cause objectionable brightness changes across the the aligned edges.

A preliminary trade-off, performed during the proposal effort for this program, between these two approaches lead to the preliminary selection of the single lens system. The primary reason for this decision was the nonuniform brightness of the four-lens approach.

A more detailed trade-off study between the two alternatives was performed at the start of this program. One significant result of this study is illustrated in Figure 23, which shows the apparent brightness as a function of position across the diagonal of viewing screen of the single lens projection display shown in Figure 22a. The brightness is shown for screen gains of five and fifteen, and for viewing positions on the display axis (solid line) and 1.5 inches to the side of the display axis (dashed line). As would be expected due to symmetry, there are no apparent discontinuities in the brightness curves for on-axis viewing. However, when viewed from 1.5-inches off axis, a step change in brightness appears at the center of the display. The magnitude of this brightness discontinuity would force the use of a screen with a gain of no more than five.

The same sort of brightness steps would occur, to a greater extent, in the four-lens system. However, neither system is acceptable except with a very low screen gain, and an improved screen structure would have to be developed for either alternative four-module display concept.

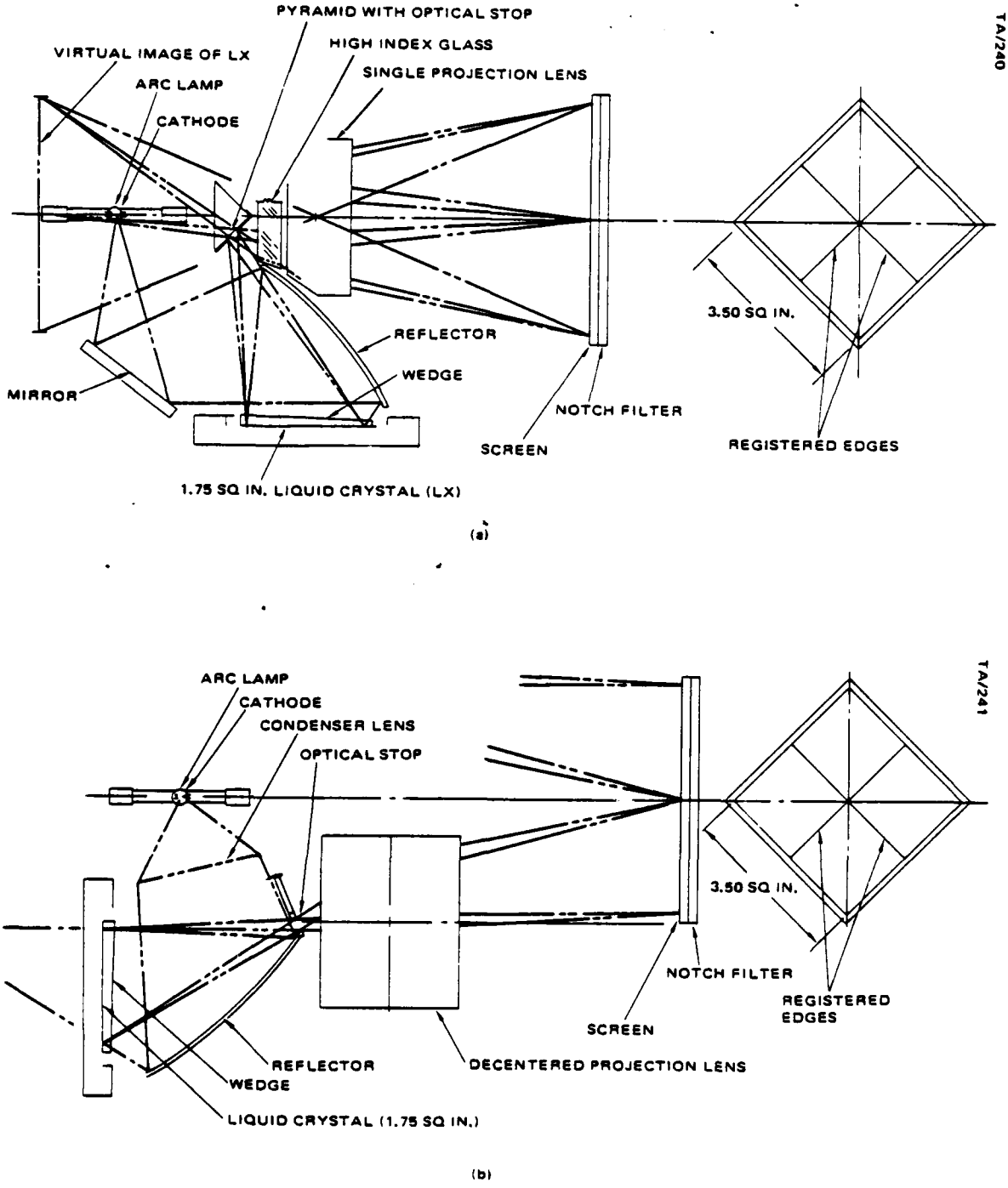


Figure 22. Alternative four module projection display concepts.

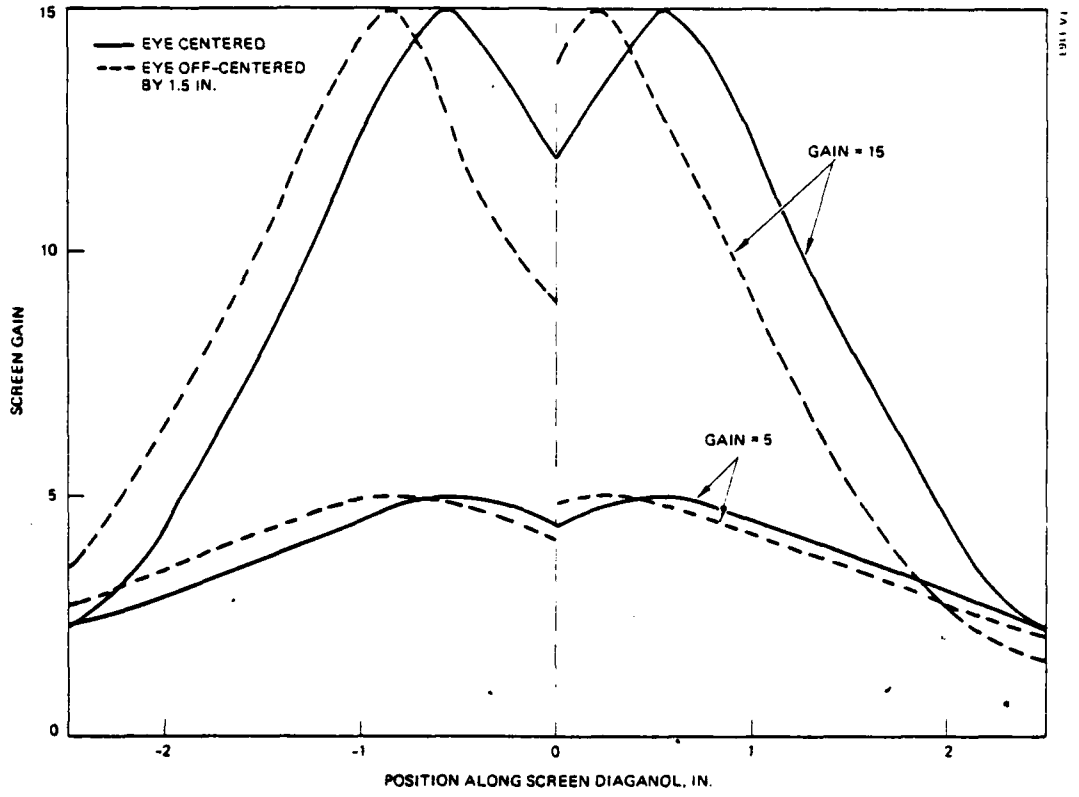


Figure 23. Brightness uniformity of four-module single lens projection display.

Thus, in order to proceed with either four-module display approach, the major problem of brightness discontinuities at the aligned edges had to be overcome. As will be described in a subsequent section, this problem was solved through the use of a homogeneous high gain screen with a four piece, Quad fresnel lens structure which would bend the incident rays from the projection system closer to each other. This lens assembly not only smoothed out the discontinuities, but it also had a positive effect on the overall brightness uniformity and allowed the use of a high gain screen without hot spots.

Given the realization that brightness uniformity was not a significant difference between the two alternatives, the four-lens approach was selected for three reasons. First, the design of a single projection lens was considered a greater risk than the design of four matched projection lenses. This is not to say that the design can not be done, but for a first run demonstration, the second approach was adequate. Second, the demonstration of the optical combining of four separate images was to be on an optical bench. The compactness of the first baseline approach was not adaptable to "off-the-shelf" mechanical fixtures. Third, and most significant, the demonstration of

a four-module projection display using discrete projection lenses for each display module would lead directly to higher resolution displays with more than four modules.

The optical design for the four module projection display can be separated into four functional sections as follows: the projection optics, the lamp house including the lamp and the condensing (light collecting) optics, the aperture, and the Quad fresnel lens screen. Figure 24 illustrates the relative positions and functions of each of the sections.

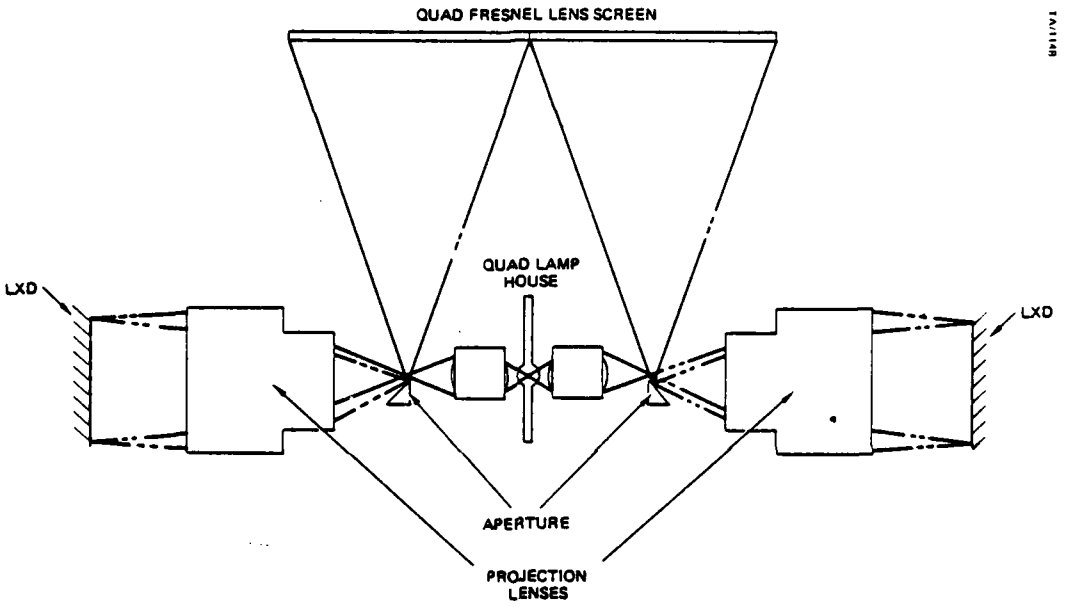


Figure 24. Projection system optical layout.

2. PROJECTION OPTICS

The projection optics in a specular mode liquid crystal projection display must perform a dual function, as shown in Figure 25. The projection lens must form an image of the liquid crystal module at the screen with the high image quality and low distortion required to align the four separate images. Additionally, the projection lens must collimate the light from the lamp house and direct it towards the liquid crystal display module. Upon reflection from the liquid crystal module, the projection lens must refocus the light to a point without introducing aberrations that would prevent the specularly reflected rays from passing through the aperture.

Initial single module experimental projectors constructed on this program used "off-the-shelf" projection lenses. These systems had reduced optical performance and excessive distortion because the stock lenses were not designed specifically for the two roles they were required to perform. The

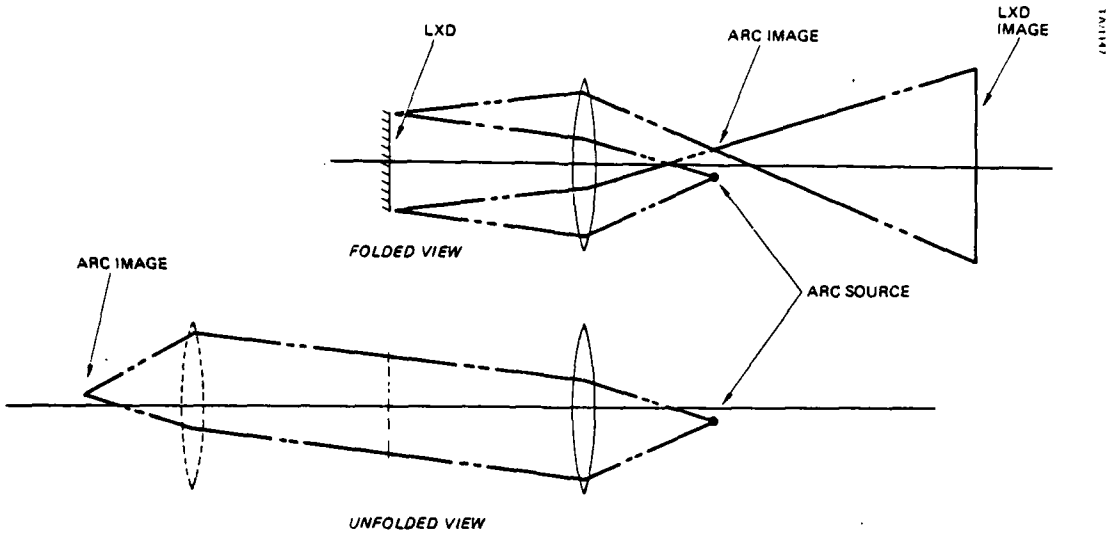


Figure 25. Dual functions of projection lens.

projection lenses used in the optical bench four-module projection display were designed by computer ray-tracing and optimizing procedures specifically for this application.

A total of four projection lens designs were considered for the use in the optical bench Quad. All were optimized to produce the least distortion for their own given scale of complexity. Three of the designs had three lenses between the LXD and the aperture, while the fourth design incorporated two additional lenses between the aperture and the screen. Figure 26 compares the relative physical sizes of the four systems.

Geometric distortion is defined as the difference between the position of an off-axis image point and its theoretical paraxial position. The two fundamental types of distortion, positive, or "pin-cushion" distortion and negative, or "barrel" distortion, are shown in Figure 27. The displacement of the corners, either in or out from the nominal edge, is due to the fact that distortion usually increases with the cube of the image height. Since the corners are further from the center than the edges, they are more grossly displaced from their paraxial position, hence giving an appearance of a "pin-cushion" or a "barrel".

In the design of the four module projection display, however, the absolute distortion described above is not as important as the net distortion along the edges. Net distortion is the difference between the distortion at the center of the edge and the distortion at the corner. When two such images are brought into alignment, such as in the four module projection display, the net distortion will determine the actual gap size between the two images. Moreover, since only two edges of each image are used for alignment (the other

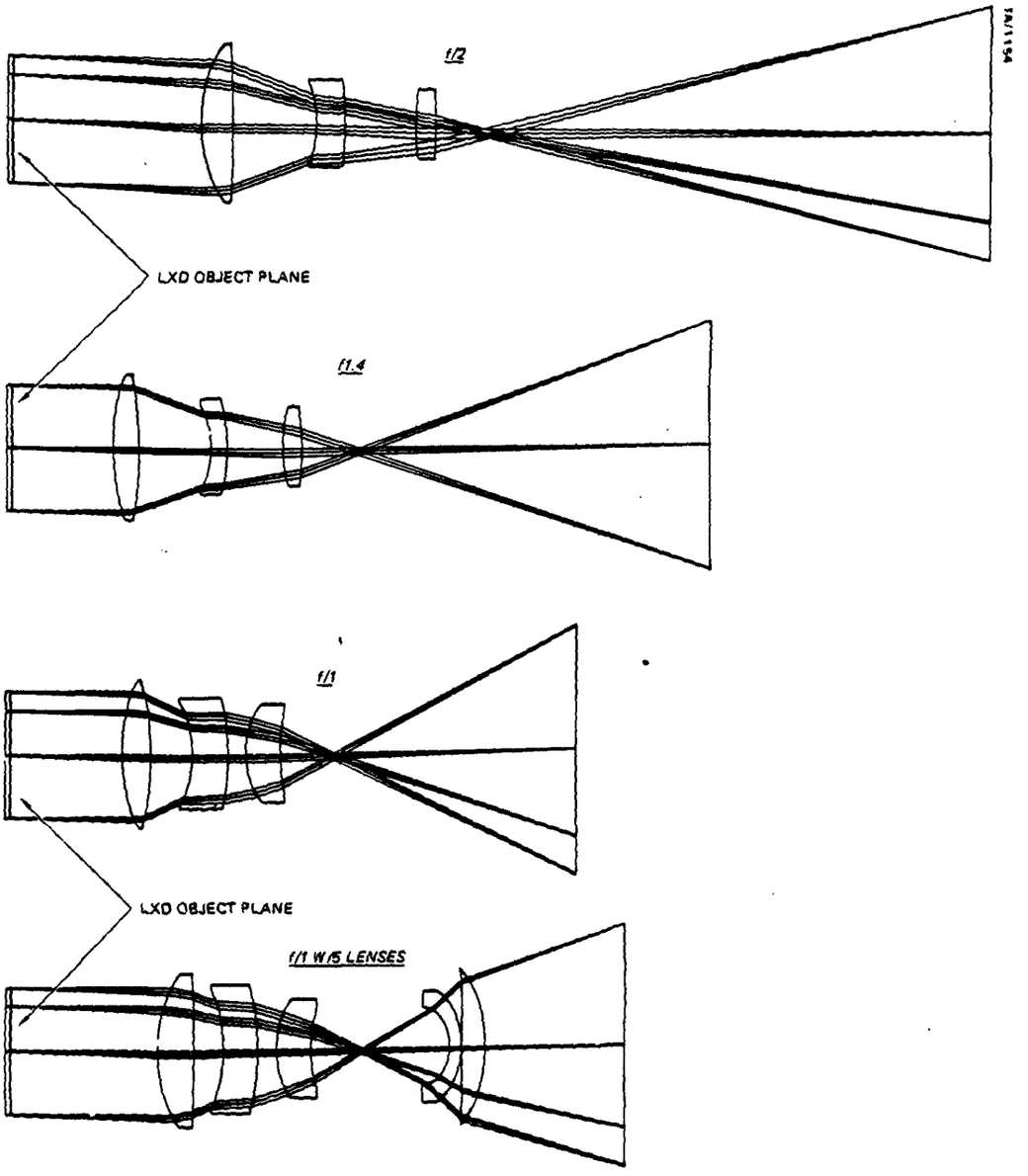


Figure 26. Four alternative projection lens designs.

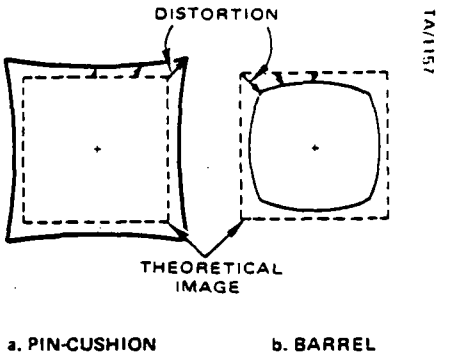


Figure 27. Distortion of projected images.

two represent the outer edges of the display), only these edges require low net distortion. Low net distortion on three or four edges will be required in future applications using more than four liquid crystal modules.

Image distortion is inherent in any nonsymmetrical optical system. Two methods are available to the designer to reduce the net distortion along the edge of the image. The first method is simply to reduce the speed of the optical system. Reducing the system speed has the effect of bringing the off-axis chief ray closer to the theoretical paraxial chief ray. This effect results in less overall distortion but necessarily increases the optical path length of the system. The second method is to use higher-order distortion terms to correct the regular third-order (cubic) distortion. By adding lenses between the aperture and the screen, distortion of the opposite polarity can be use to cancel the distortion of the lenses between the liquid crystal modules and the aperture.

Figure 28 plots the net distortion along the edge of the image for the four projection lenses designed on this program. The three-element f/1 and f/2 lenses are examples of third-order distortion producing a "barrel" image. The five-element f/1 lens is an example of the use of higher-order terms to correct the distortion near the corners of the image. The f/1.4 design is a compromise between the excessive distortion of the f/1.0 lens and the length of the f/2.0 design. Note that the distortion curve for this design is not symmetric. This design took advantage of the decentered aperture to decrease the distortion on the sides of the image which must be aligned at the center of the display.

The tradeoff established in comparing the four designs was one of complexity, optical path length, and overall speed versus geometric distortion. Table 14 lists each design along with its appropriate speed, path length, number of lenses (complexity) and net distortion along the aligned edge.

The choice of the f/1.4 design was based on the need for a design with low enough net distortion to demonstrate optical image alignment and the constraints of "off-the-shelf" optical bench apparatus. The minimal net

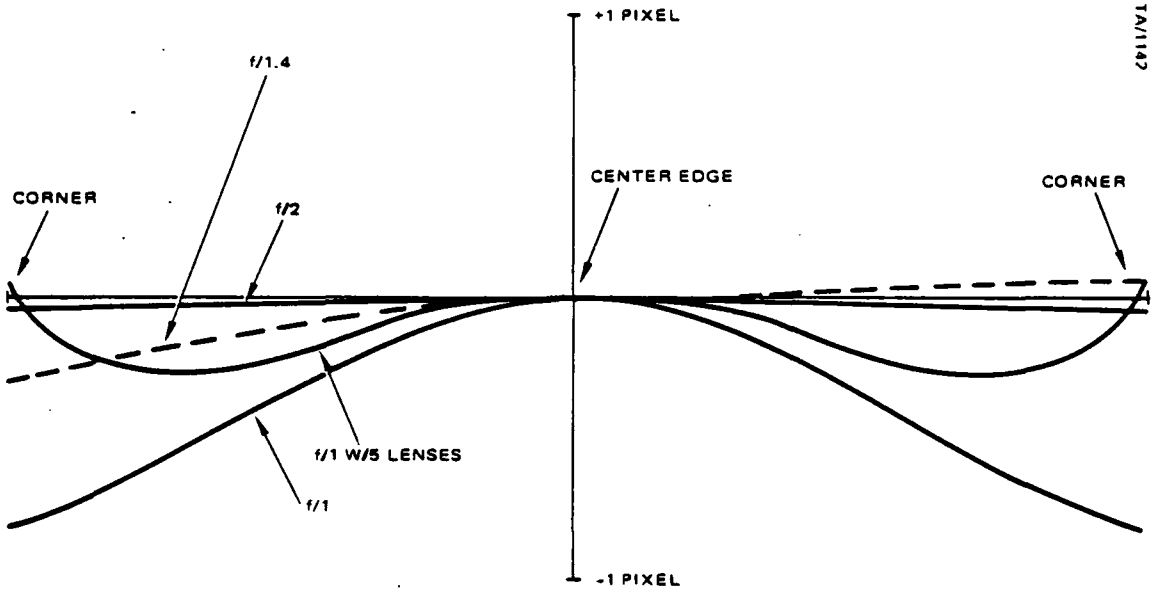


Figure 28. Distortion of alternative projection lenses.

TABLE 14.

COMPARISON OF QUAD OPTICAL DESIGNS

DESIGN	PATH LENGTH	# OF LENSES	GAP SIZE*
f/2	19.1"	3	.080
f/1.4	13.9"	3	.60
f/1	11.3"	3	1.60
f/1	12.1"	5	.52

* GAP SIZE is the largest net distortion between two aligned images, effectively double the individual image distortion. The size is expressed as a fraction of the size of an element on the projected image.

distortion allowable in the Quad image is related to the eye position (exit pupil distance to screen) and the contrast between the gap and the bright edges. Given a distance of 30 inches from the eye to the screen, one pixel would subtend approximately 2 minutes of arc. The visual acuity of the eye is

accepted to be about 1 minute for a situation of high contrast as is the case of the dark gap surrounded by the bright LXD images. Therefore, an acuity of 1 minute translates into a maximum net distortion of approximately .5 pixel gap.

In order to keep the optical path length within reason ((15"), only the f/1.4 and the five-element f/1 lens designs met the distortion requirement. The five-element f/1 lens had less net distortion and a shorter optical path length, but could not be constructed using the available standard optical bench fixtures due to interference between the two lens elements after the aperture and the lamp house. Therefore, the three-element f/1.4 design was selected as the alternative which best satisfied all of the objectives of the optical bench four-module projection display.

The image coordinate system used to describe the performance of the f/1.4 lens design is shown in Figure 29, and described in Table 15. This table also list the calculated brightness uniformity across a single display quadrant. The uniformity is easily better than the 2:1 brightness variation generally considered to be the point where the eye begins to detect differences in intensity across a display surface.

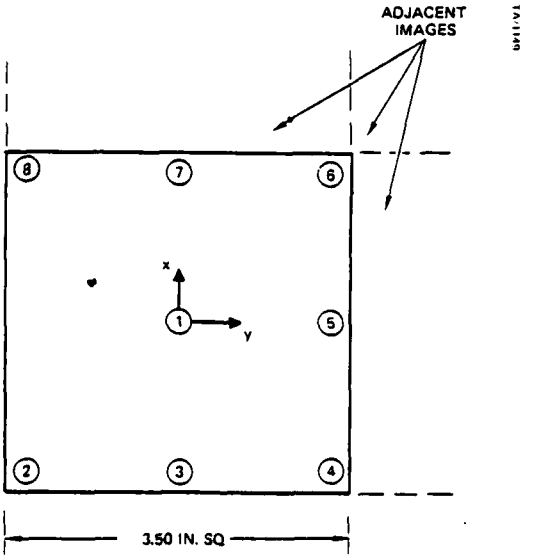


Figure 29. Image test point locations.

Figure 30 shows the overall distortion and field curvature of the system. The net distortion varies along the edges that will be combined at the center of the four module display. The gap between the adjacent quadrants of the image will be 0.1 element in width at the very center of the display and increase to 0.6 element at the extreme edges. The distortion on the outer edges is as high 0.8 element, due to the decentered nature of the optical system. The field curvature plot indicates that the best compromise focus position is about .25 inches shorter than the paraxial focus and that the image curvature is within 0.5 inch.

TABLE 15.

IMAGE PLANE COORDINATES

POINT	LOCATION	X	Y	% ILLUMINATION
1	Center	-.002	-.002	100
2	Corner	-1.750	-1.750	74
3	Edge	.0013	-1.751	
4	Corner	1.752	1.743	73
5	Edge	1.751	.002	85
6	Corner	1.745	1.745	75
7	Edge	.002	1.751	85
8	Corner	-1.743	1.752	73

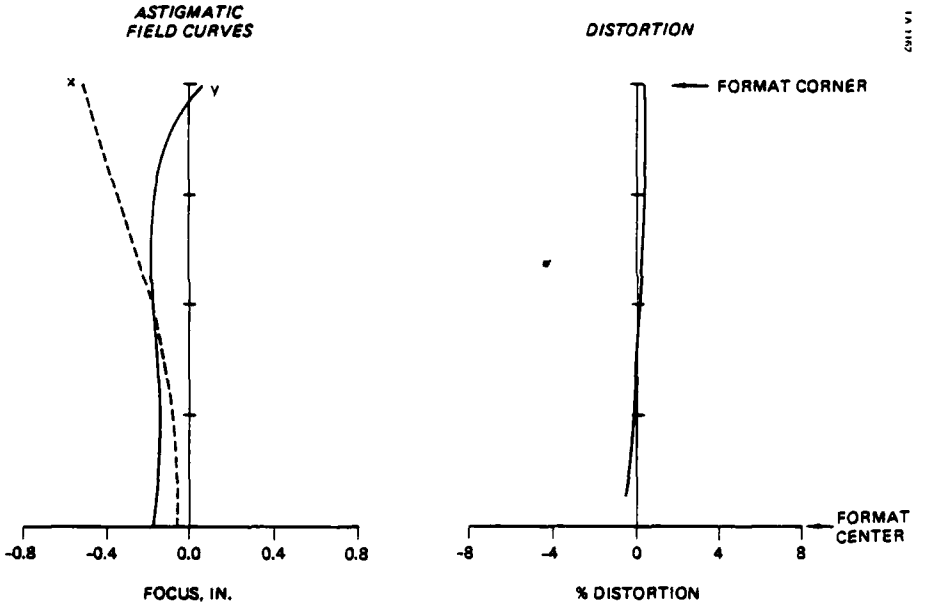


Figure 30. Projection lens field curvature and distortion.

The blur spot size and overall modulation transfer function (MTF) are shown in Figures 31 and 32, respectively. Given a point on the LXD object surface, the corresponding point on the image plane will be blurred by the amount shown in Figure 31. Note that the blur sizes are all less than .5 pixel in size, which is the limit of the eye's visual acuity, and hence is not overly noticeable. The MTF's for different areas in the image plane are all diffraction limited for bar patterns with a spatial frequency of 0.5 cycle per display element (alternating bright and dark elements).

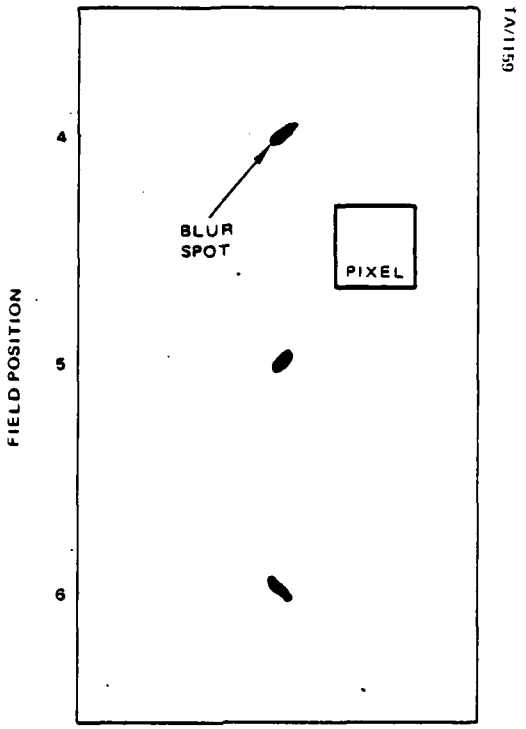


Figure 31. Blur spot size at three image test points.

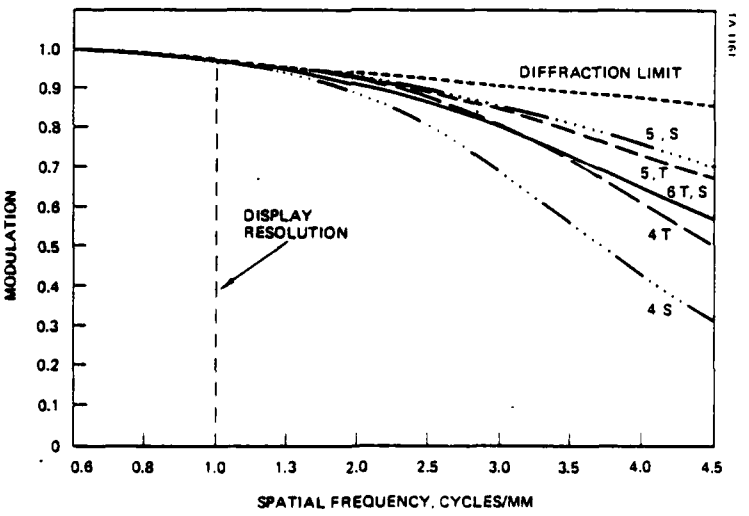


Figure 32. Image modulation transfer function.

3. LAMP HOUSE

Both of the initial four-module projection display concepts shown in Figure 22 used ellipsoidal reflector condensing optics (light gathering optics around the illumination source). This type of reflector had been used in previous single-module projection display designs (such as the Integrated Head-Up Display) because it maximizes the amount of light collected from the lamp for illumination of a single display module. The aberrations of the ellipsoidal reflector do cause significant variations in brightness across the projected image.

The condensing optics for a four-module display are placed on four sides of the illumination source. The total amount of light that can be collected is limited by mechanical constraints and reflective optics do not provide any advantage over refractive (glass lenses) optics. Refractive condensing optics offer the advantages of more uniform illumination of the liquid crystal modules, lower cost (particularly if stock items can be used), and greater compatibility with standard optical bench fixtures. Glass condensing optics were selected for use in the four-module projection display.

The lamp house for the optical bench four-module projection display demonstration system was composed of a 100 watt mercury-vapor arc lamp surrounded by four sets of condensing optics. Figure 33 shows the key components of the lamp house, viewed from the top along the axis of the lamp.

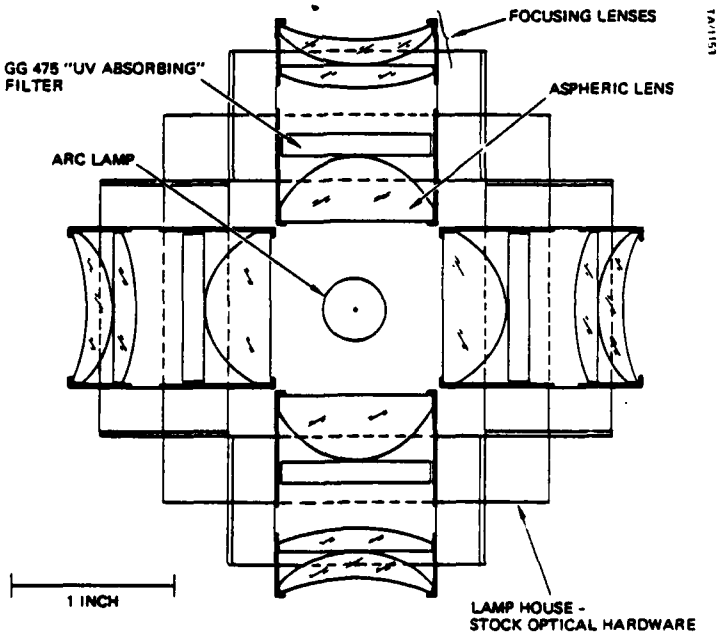


Figure 33. Top view of lamp house.

The mercury vapor lamp produces 2200 lumens emanating from a spherical arc approximately 0.25 millimeter in diameter. Of the 2200 total lumens, greater than 50% is contained in the 546 and 578 nanometer principle lines, as shown in the spectrum of a mercury source in Figure 34. This particular lamp was selected for three reasons. First, the small size of the arc was required to ensure the passage of the specularly reflected light from the display through the system aperture. Second, the narrow spectral bandwidth of the lamp's output is compatible with future head-up displays systems which will use diffraction optics combining elements. Third, the narrow spectral output simplifies the design of low distortion projection lenses, since freedom from chromatic aberrations is not required.

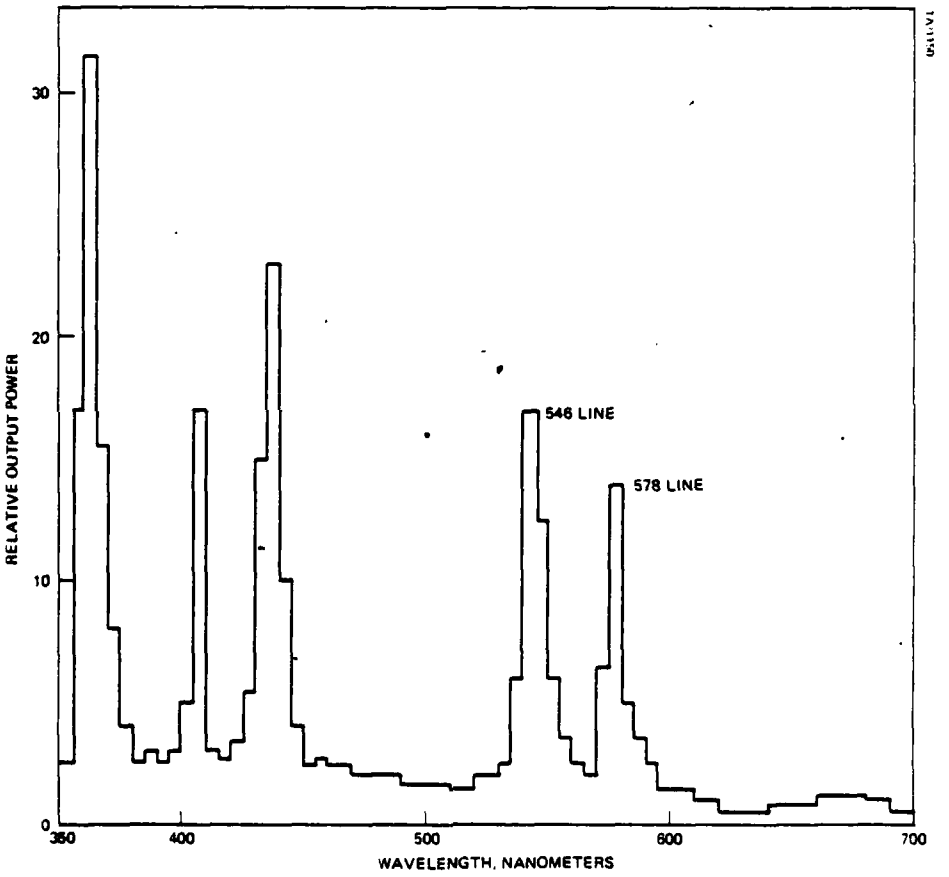


Figure 34. Spectrum of output from mercury vapor lamp.

The condensing optics was composed of an aspheric collection lens, a GG 475 Schott Glass filter, and two focusing lenses, all of which were "off-the-shelf" components. The first lens, which collects and collimates the light from the lamp, is a fast 18 millimeter focal length f/.80 aspheric lens which was capable of collecting 11.3% of the light from the arc lamp. Four such lenses symmetrically arranged around the lamp collect a total of 45% of the

lamp emission. The GG 475 filter was used to absorb the UV-blue light ((475 nanometers) which is harmful to the liquid crystal material in the displays. The second two lenses, which focus the collimated light, are a 60 millimeter focal length plano-convex lens and a 50 millimeter focal length meniscus lens. This combination produces a cone of light slightly larger than the f/1.4 cone accepted by the projection lens. The ray trace of the lamp and condensing optics is shown in Figure 35.

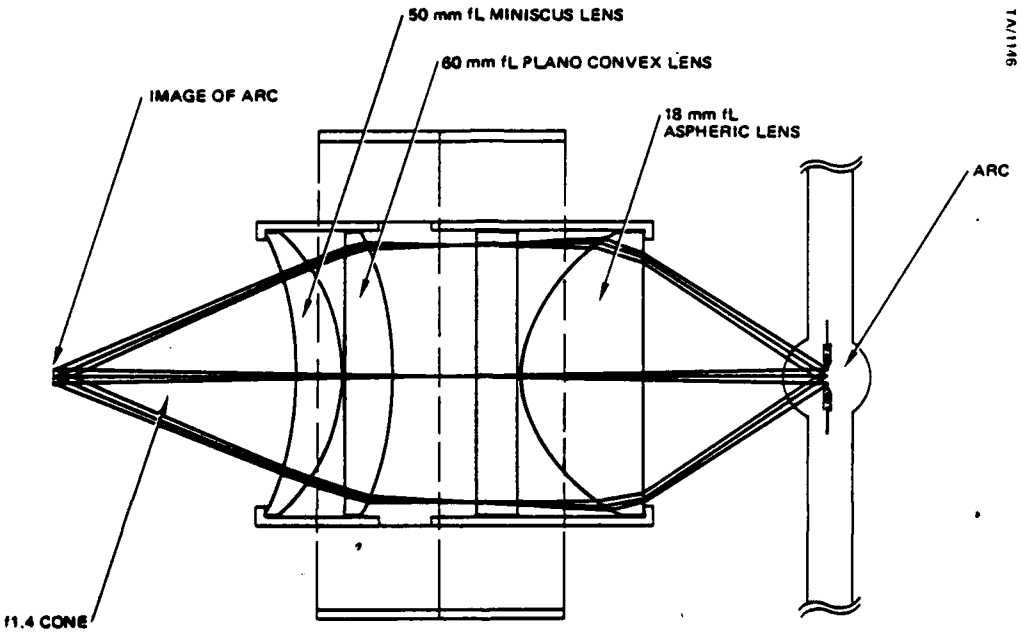


Figure 35. Lamp house optical design.

4. APERTURE

The projection lens was also optimized to collimate the light from a point source (actually an image of the lamp arc formed by the condensing optics) and then to focus the collimated light reflected from the liquid crystal module. Optical principles and test data on numerous displays were used to determine the aperture size which produces the maximum contrast ratio. First order optical principles show that, for a given lamp arc size, the maximum projection display contrast ratio is obtained when the image of the arc just fits the size of the aperture. To increase the contrast ratio further, the size of the arc necessarily has to be decreased in size. Figure 36 demonstrates the first-order effects of aperture and arc size on contrast ratio.

Test data on liquid crystal modules in simulated projection display optical systems show that a small amount of specular-state scattering does exist, and that an arbitrarily small arc and aperture will not produce the

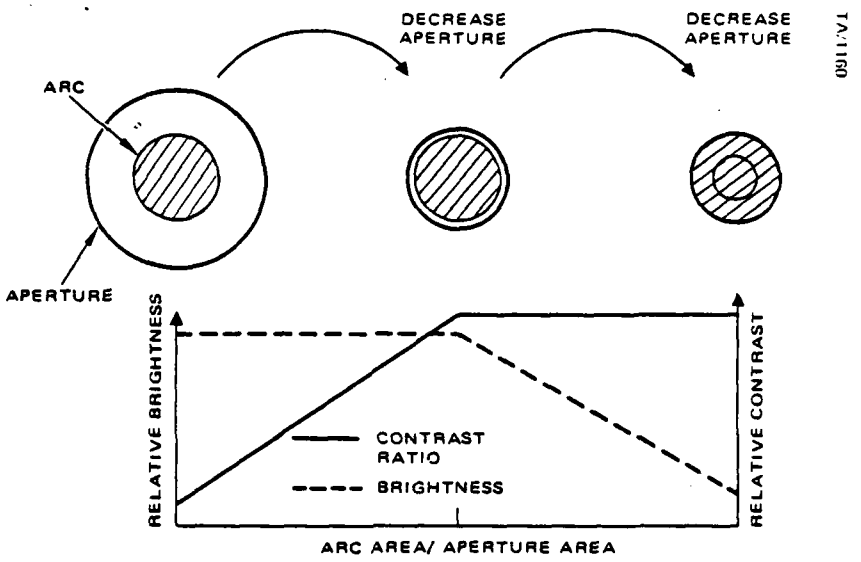


Figure 36. Effect of aperture size on brightness and contrast.

highest contrast. This slight scattering increases the size of the image of the arc formed by the projection lens, and the aperture size must be increased accordingly. For smoothed displays, an aperture which has an angular subtense (viewed from the liquid crystal module) slightly larger in diameter than that of the lamp arc is necessary to obtain maximum projection display contrast.

The arc lamp and condensing optics previously described form an image of the arc (in front of the projection lens) which subtends 2.0 degrees to the liquid crystal module. Display test data indicates that the maximum contrast for this display can be obtained with an aperture which subtends two and a half degrees. Formula (1) shows the relationship between aperture size,angular subtense, and projection lens focal length, and Figure 37 diagrams how this formula is derived for basic LXD projection systems.

$$\text{aperture size} = 2(\text{focal length})\tan(\text{scattering angle}/2) \quad (1)$$

The focal length of the f/1.4 projection lens is 3.5 inches. Using formula (1), the aperture diameter was calculated to be .153 inch. Since the aperture plane in the system is not parallel to the display but is cocked by 45 degrees to direct the light to the overhead screen, the actual aperture shape is 45 degree ellipse where the minor radius is still .153 inch and the major radius is .216 inch.

The construction of the aperture was accomplished by using the outside surface of the hypotenuse of a 45 degree prism. The hypotenuse was coated with aluminum and protected with a black paint covering. A properly sized elliptical hole was cut in a piece of self-adhesive paper and placed over the black surface. A cotton swab, dipped in acetone, was used to remove the paint from the exposed area leaving the rest of the black paint intact. The paper sticker was removed when the hole in the aperture/mirror had dried. The prism design is shown in Figure 38.

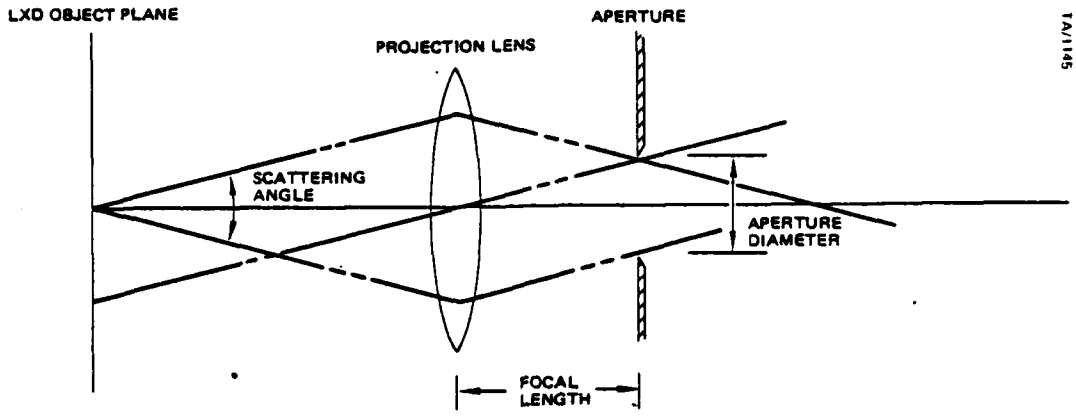


Figure 37. Determination of aperture subtense.

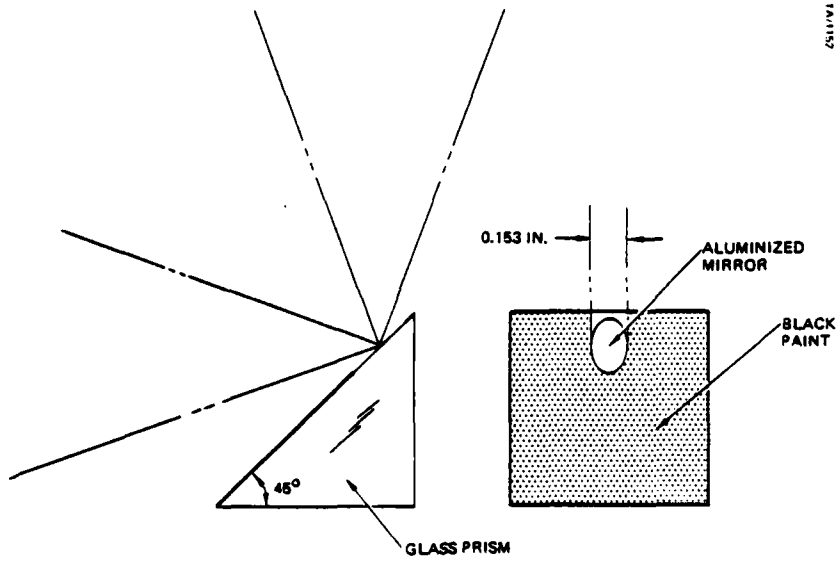


Figure 38. Aperture mirror design.

5. PROJECTION SCREEN/FRESNEL LENS ASSEMBLY

The light reflected from the aperture mirror is directed upwards towards the rear projection screen. Since the aperture is small with respect to the aperture-screen spacing, each point on the screen is illuminated by a very narrow cone of light. Additionally, the angle of incidence of the light onto the screen varies across each quadrant of the display, and there is a sharp discontinuity in the incidence angle at the junctions of the quadrants. The screen must diffuse and redirect the incident light to form a large, uniform, viewing pupil.

A variety of diffusing materials were considered for use as the projection screen. Without exception, all of these materials offer a trade-off between gain or brightness, brightness uniformity, and viewing pupil size. Figure 39 compares the brightness distributions of diffuse light from two common diffusing materials, ground glass and opal glass.

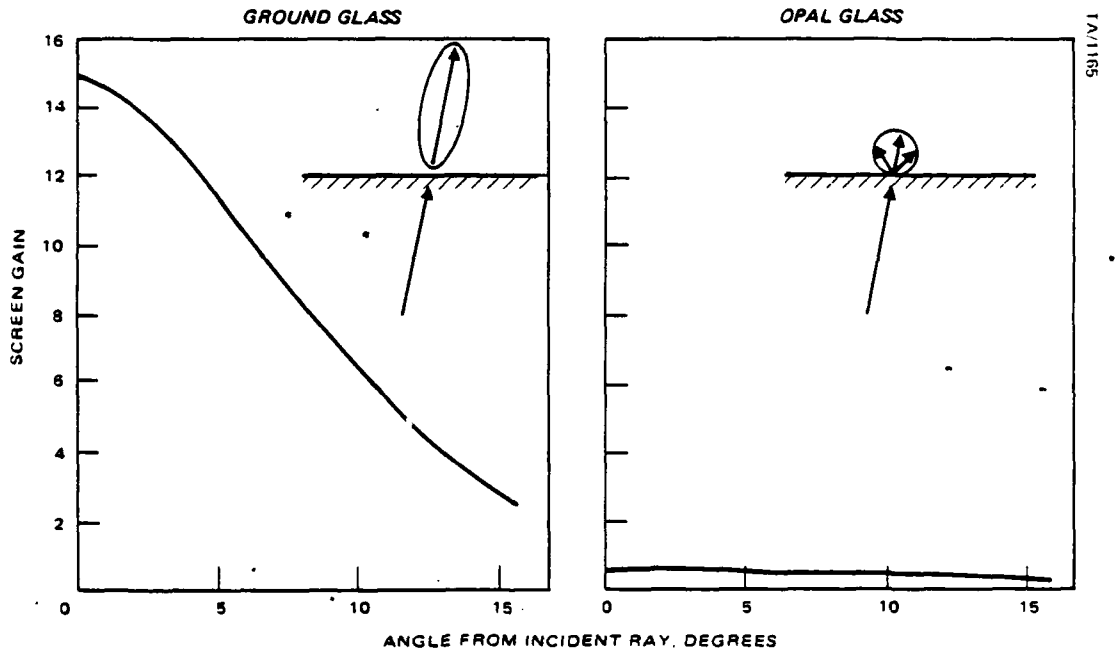


Figure 39. Gain versus viewing angle for two screen materials.

Opal glass appears the same brightness from all angles of viewing but has low gain. Ground glass, on the other hand, must be viewed exactly along the direction of the incident light in order to achieve maximum gain. The brightness decreases rapidly as the viewing angle moves away from the direction of the incident light. A projection screen material is generally selected to produce a 2:1 center to edge brightness change when viewed from the nominal eye position. As previously discussed, the discontinuity in incidence angles at the aligned edges of the four quadrants can cause an

objectionable brightness change. Thus, the general 2:1 center:edge brightness rule is not a sufficient design criterion for the screen in a four-module projection display.

The high gain of ground glass is necessary to achieve the high brightness desired for the optical bench Quad. However, a simple ground glass screen will not produce the brightness uniformity required across the aligned edges and the overall screen. Figure 40a and -b illustrate the the problem with ground glass alone as the diffusing medium. Given an exit pupil (the eye position) in the center of the screen, the gain of the ground glass screen is only maximized in the one viewing direction along the ray from the aperture to the eye. Since each quadrant has its own aperture, there are in effect four separate high brightness areas, known as "hot spots", which produce overall brightness nonuniformities.

Since the incidence angles at the aligned edges of the quadrants are symmetric about the viewing direct, there are no sharp brightness changes along these edges for the centered eye position. For other eye positions, as shown in Figure 40b, there is an objectionable discontinuity between the brightnesses of adjacent quadrants. The eye is sensitive changes in brightness along edges and any brightness discontinuity must be avoided.

The solution to four-module display uniformity problem is accomplished with the use of four aligned fresnel lenses. The action of the lenses is to bend each diffuse cone of light towards the nominal eye position such that all positions on the screen appear equally bright. The effect of the fresnel lenses on screen performance is shown in Figure 40-c and -d. The brightness nonuniformity caused by the directional properties of the ground glass is all but eliminated for the eye in the center position (nominal exit pupil). The only remaining large area brightness changes are caused by the optical system and are much less than the maximum tolerable 2:1 difference.

The fresnel lenses are designed such that the incident rays on either side of the aligned quadrant edges are directed perpendicular to the ground glass diffusing screen. Since these rays now impact the diffusing surface at identical angles, there are no brightness discontinuities, even when the eye moves to either side of the designed central exit pupil. The small dip in brightness at the aligned edges is due to the thickness of the fresnel lens, which creates a subtle shadowing situation, and to slight alignment errors. Figure 41 shows details of the fresnel lens design.

The fresnel lenses were designed to define an exit pupil approximately 40 inches from the center of the screen. Since the aperture-to-screen distance was seven inches, an off-the-shelf fresnel lens with a focal length of six inches was selected. Each fresnel lens was cut into a square the size of the magnified image quadrant in such a way as to put the center of the fresnel rings in line with the aperture and the nominal eye position.

In addition to resolving the brightness uniformity problem, the fresnel lens assembly also help to reduce extraneous images caused by light reflected from the borders of the liquid crystal display modules outside of the active

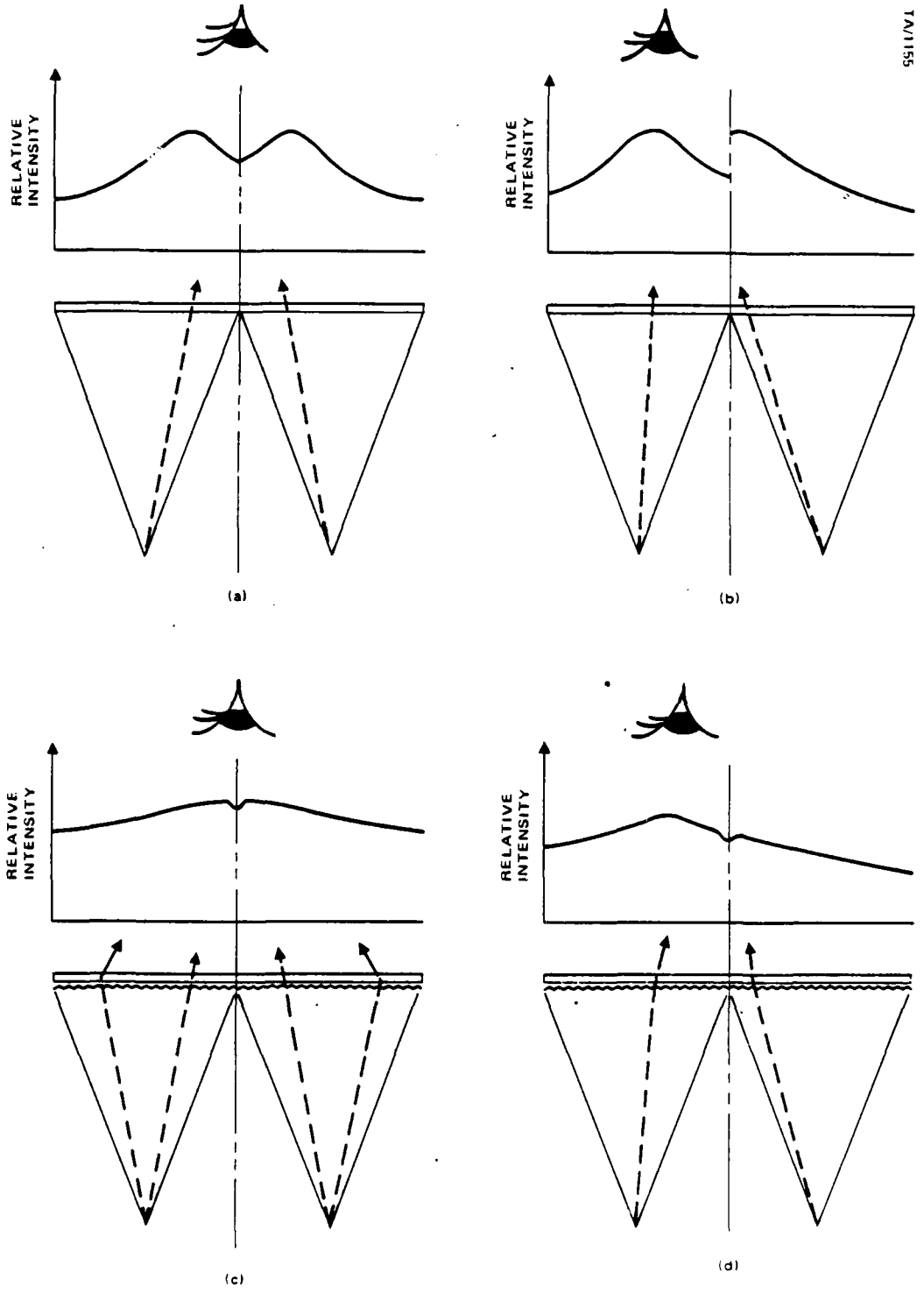


Figure 40. Image brightness uniformity with and without fresnel lenses.

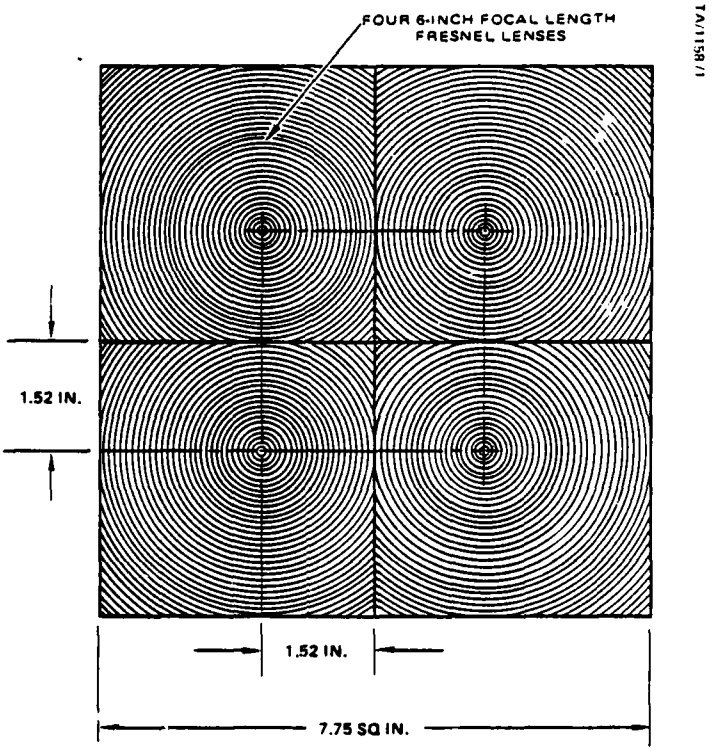


Figure 41. Fresnel lens assembly design.

image area. As shown in Figure 42-a, without fresnel lenses, light that is specularly reflected from nonactive areas of the liquid crystal modules reaches the screen and is superimposed on the images of the adjacent display quadrants. This light degrades the picture quality and contrast ratio.

A simplistic approaching to solving this problem would be to place opaque masks around the perimeter of each liquid crystal module to block the incident light. However, the liquid crystal modules are constructed with a glass cover and an ultraviolet absorbing filter on top of the liquid crystal layer. Thus the opaque mask is located .25 inch above the module image plane, and accurate masking is difficult.

As illustrated in Figure 42b, rays from the nonactive areas of the liquid crystal module are incident on the fresnel lens of the adjacent display quadrant and are deflected away from, rather than towards, the nominal eye position. Only a small fraction of the unwanted light reaches the observer's eye, and there is no noticeable degradation of the displayed image. These stray reflections are visible from well outside the normal exit pupil. This phenomenon can be easily viewed by moving the eye in and out of exit pupil, watching the stray light disappear and reappear. Since most of the stray light is optically removed from the image, accurate masking techniques were not needed and easily applied tape masks were used.

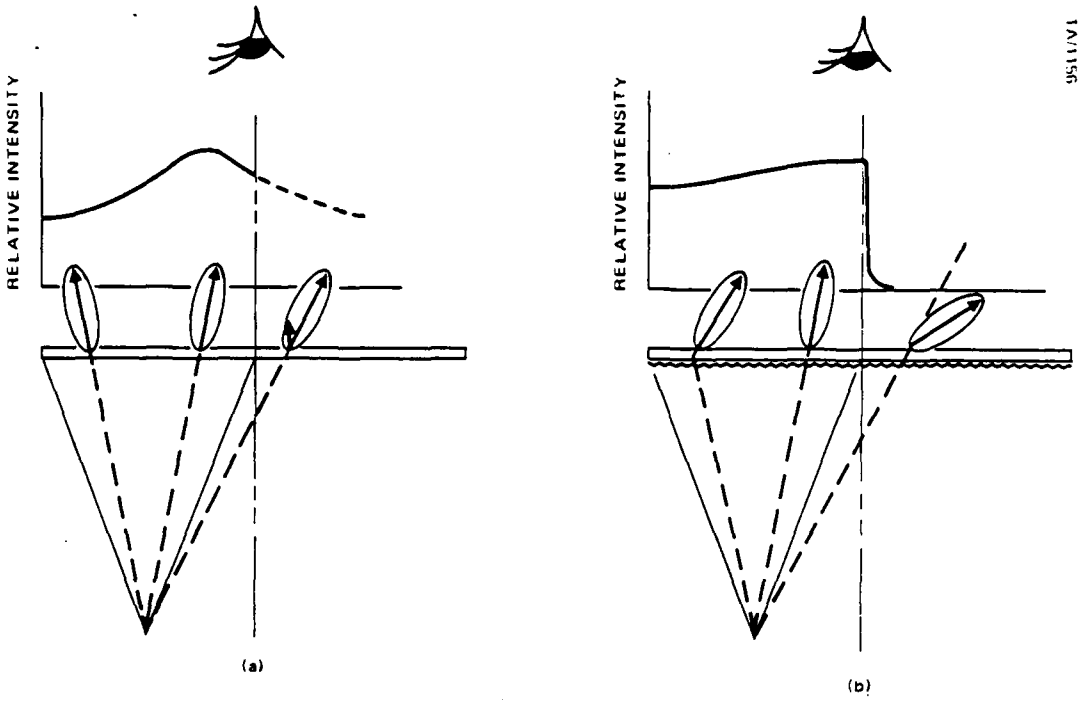


Figure 42. Fresnel lens assembly rejects undesired stray reflections.

SECTION V.

PROJECTION DISPLAY CONSTRUCTION/PERFORMANCE

1. PHYSICAL DESIGN

The physical design of the four-module projection display was based on the use of stock optical bench components when ever possible. The structural layout of the optical bench Quad was composed of the Quad Lamp House supported by standard rods, four interchangeable projection display units, and a screen-mirror assembly. A photograph of the completed four-module projection display was previously shown in Figure 5 and is repeated in Figure 43.

Each of the four interchangeable projection display subassemblies is constructed on an optical bench rail and includes an aperture-prism assembly, a three-element projection lens inside a custom lens barrel, and a liquid crystal display modules with driver electronics. A single projection display unit is photographed in Figure 44.

The f/1.4 projection lens was composed of three SF11-type glass lenses housed in a custom lens barrel. The projection lens design was computer-optimized for low distortion at the screen and small arc size growth at the aperture. A photograph of an assembled projection lens is shown in Figure 45 and a cut-away assembly drawing is shown in Figure 46.

Part of the lens design process included establishing manufacturing tolerances for the lens elements and the spacers within the lens barrel. Mechanical tolerances for thicknesses, curvature, overall tilt, and decenter were defined for each lens element. All of these parameters could adversely affect the quality of the performance of the lens group. Similarly the thicknesses and diameters of the lens barrel and spacers were toleranced so as not to significantly add to the lens errors. Additional cross tolerances were defined between the four lens assemblies to ensure that each had the same focal properties for correct magnification of each quadrant.

The tolerances on the projection lens components, summarized in Table 16, were established to ensure that the illumination reflected from the liquid crystal display module could pass through the system aperture, that the MTF at one cycle/millimeter remained above .85 at all field points and that manufacturing errors would not introduce significant distortion. The computer software used in the lens design does not allow the use of spot size to directly determine tolerances. Thus the relationship between spot size growth to an increase in RMS wavefront error for a simple aberration such as focus error was determined, and the lens tolerances were established to limit the RMS wavefront error to that corresponding to the maximum spot size desired.

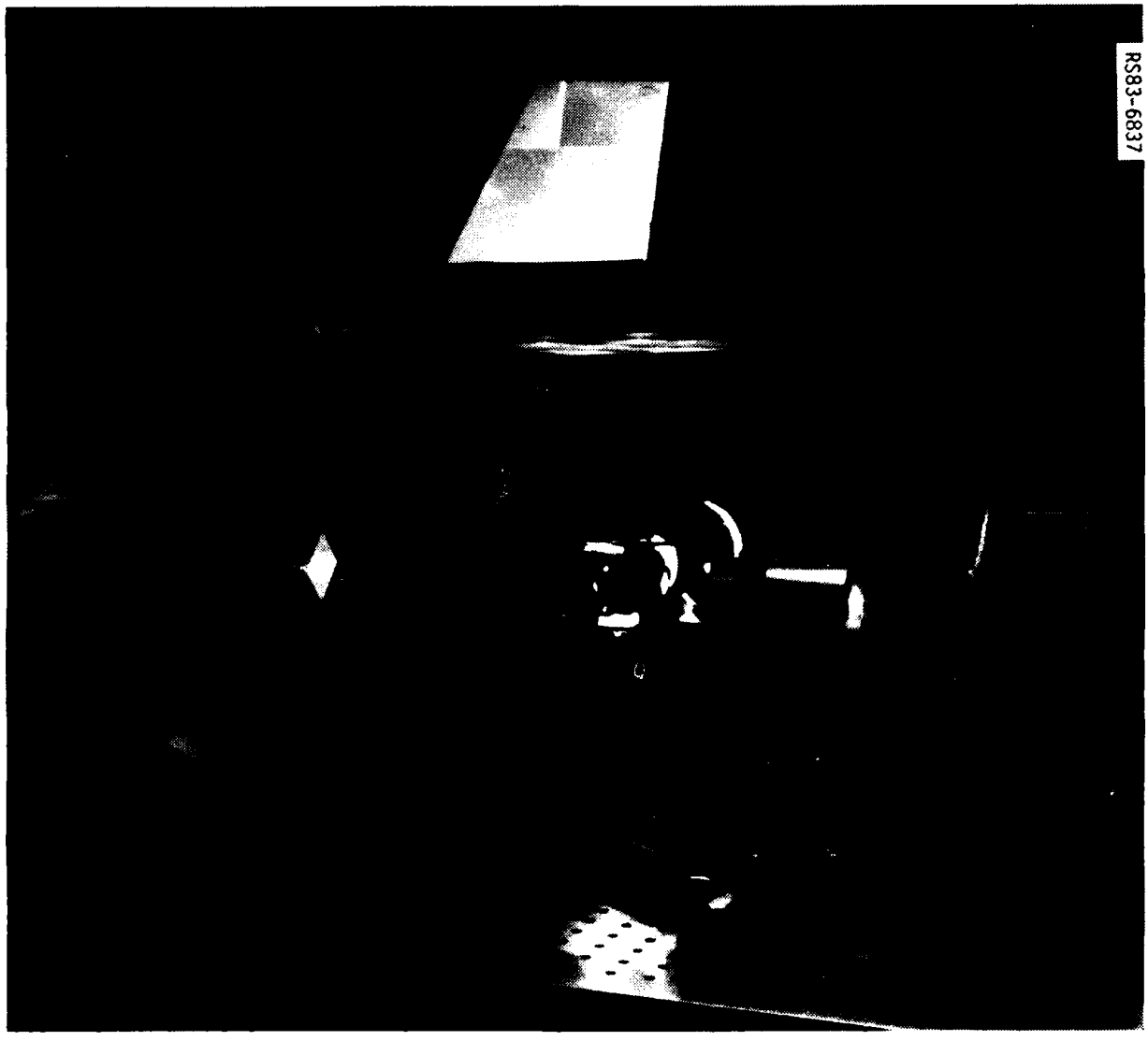


Figure 43. Optical bench model four-module projection display.

The curvatures of all lens were selected to match existing precision test plates, and the lens tolerance analysis assumed that all radii of curvature were measured and known to better than 0.5% of the actual radius.

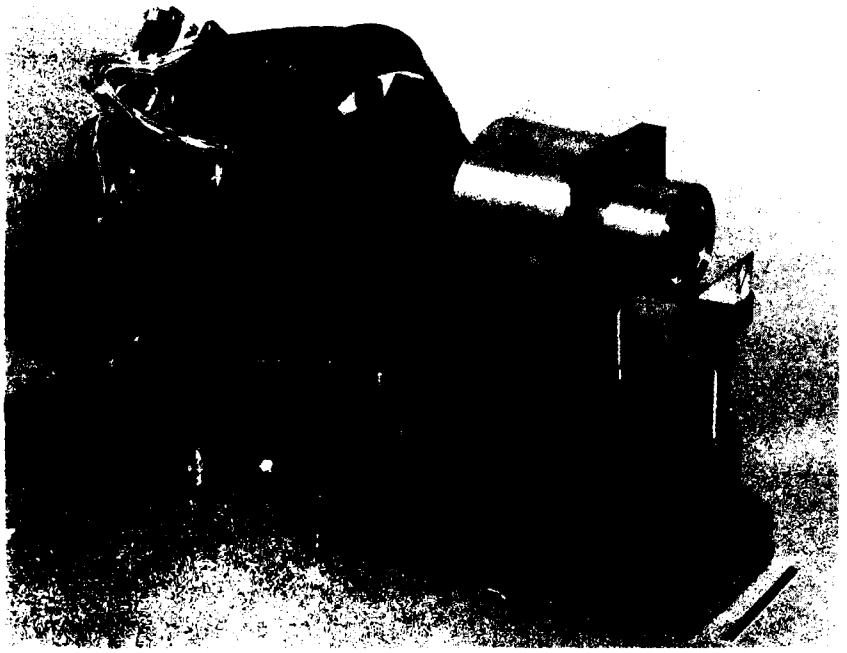


Figure 44. Projection display subassembly.

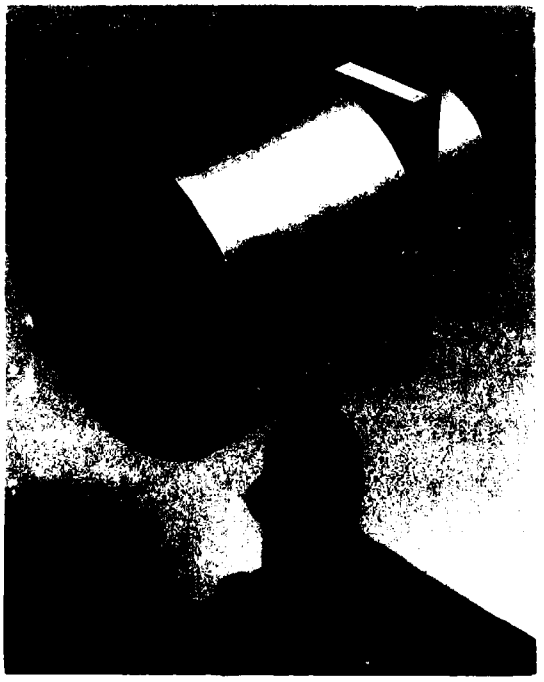
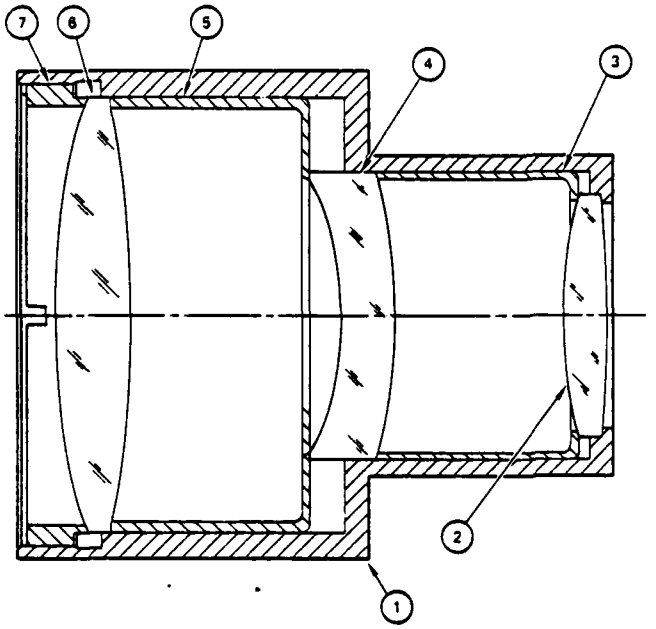


Figure 45. Assembled projection lens.



RING	7
LENS ELEMENT I	6
SPACER II	5
LENS ELEMENT II	4
SPACER I	3
LENS ELEMENT III	2
CELL	1

Figure 46. Cut away view of projection lens assembly.

TABLE 16.

PROJECTION LENS TOLERANCES

	Lens Element Number 1	2	3
Test Plate Power (1) Fringes at 546 NM	8	8	8
Test Plate Irregularity Fringes at 546 NM	2	3	3
Axial Thickness, mils	5	5	5
Axial Displacement, mils	10	4	4
Element Decenter, mils	2	3	5
Element Wedge, arc minutes	2	6.3	7
Element Tilt, arc minutes	4.1	5.2	17.2

1. Compared to precision test plate of desired radius.

The results of the lens tolerance analysis indicated that a +/- 0.05 inch axial adjustment range would be required on the aperture position. Additionally, a small adjustment of the distance between the aperture and the screen was needed to provide the same magnification in each quadrant without significant blur from defocus.

Each liquid crystal display module was supported on a multi-adjustable optical mount which provides six degrees-of-freedom : linear motion along the optical axis and two orthogonal axis along the diagonals of the display, and rotary motion around each of these axis. These mounts were selected to provide a sufficient number of adjustments to ensure that each display could be moved into alignment.

Three LSI driver circuit printed wiring boards and one interconnection board were necessary for each display. The four circuit boards were mounted behind the liquid crystal display module and securely attached to a support base. The display module/driver subassembly is shown in Figure 47. The driver circuits will be described in detail in a subsequent section.

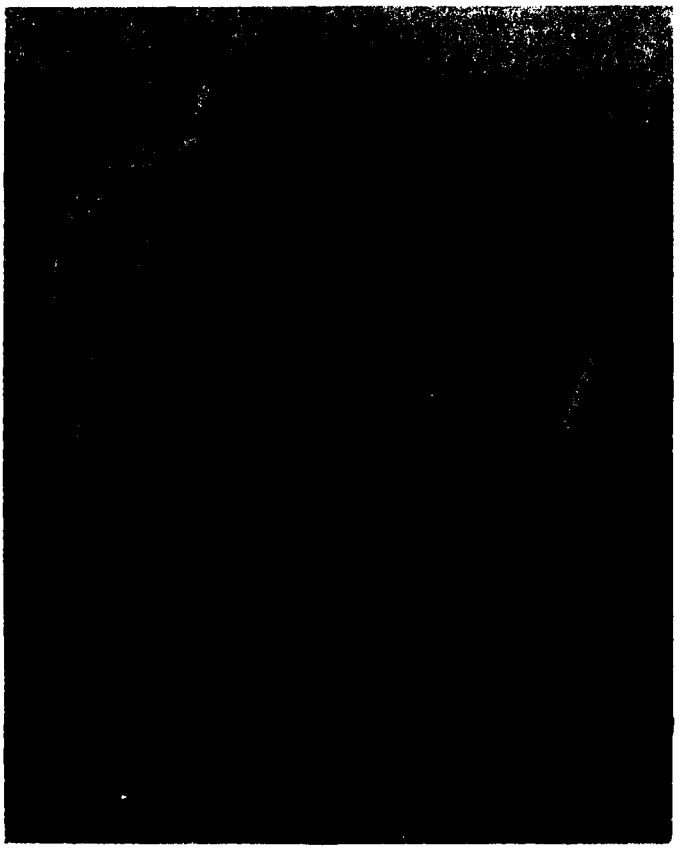


Figure 47. Driver boards mounted behind liquid crystal display module.

The lamp house, shown in Figure 48, was constructed from "off-the-shelf" miniature optical bench components which formed a small box around the arc lamp. All edges which were bolted together were first coated with a thin layer of thermal grease for better heat transfer. The condensing optics were mounted in standard lens barrels centered in the sides of the box.

Thick metal plates were used to provide electrical and thermal contact to the metallic end caps of the mercury-vapor arc lamp. Standard power transistor heat sinks were attached (along with thermal grease) to each plate to dissipate the heat from the ends of the lamp. An epoxy-glass sheet was mounted on the inner sides of the end plates to provide adequate electrical isolation between the ends of the lamp and the body of the lamp house. The four spring-loaded screws which held the upper plate to the lamp house box could be used to adjust the arc lamp's position to achieve uniform illumination into each condensing lens group.

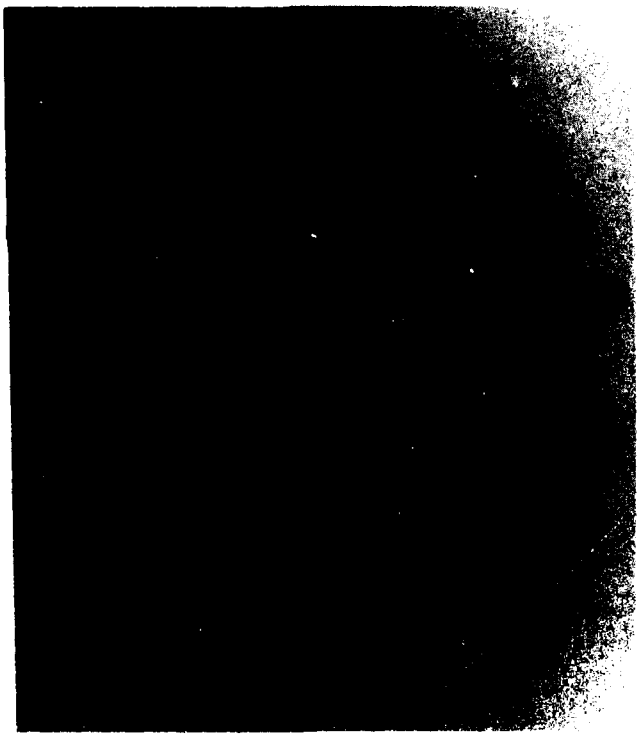


Figure 48. Lamp house.

Although the optical bench four module projection display was designed for operation in a laboratory environment only, the heat build up in the lamp house was a possible safety hazard. The temperature of various points on the lamp house was measured during actual operation. The measured temperatures are presented in Figure 49 as a function of elapsed time from lamp ignition. All exposed areas of the lamp house were within the tolerable temperature limits for safe lamp operation, and do not present a burn hazard.

The screen-mirror assembly was mounted directly above and centered about the Quad lamp house. Since the normal to the screen surface was pointed upward, a folding mirror placed above the screen was used to direct the exit pupil towards a seated observer. The screen-mirror mounting structure is shown in Figure 50.

The four-section fresnel lens assembly required fine adjustment with respect to the aligned four quadrant image. The edges of the fresnel lenses had to be aligned with the corresponding edges of the four projected images in order to produce the correct result. The fresnel lenses were aligned and glued to a ground glass screen which was, in turn, glued into a metal frame. This frame was mounted inside a larger frame which contains adjustment screws pointing in towards the screen assembly. These screws are used to move the screen until the alignment between the projected images and the fresnel lenses was achieved.

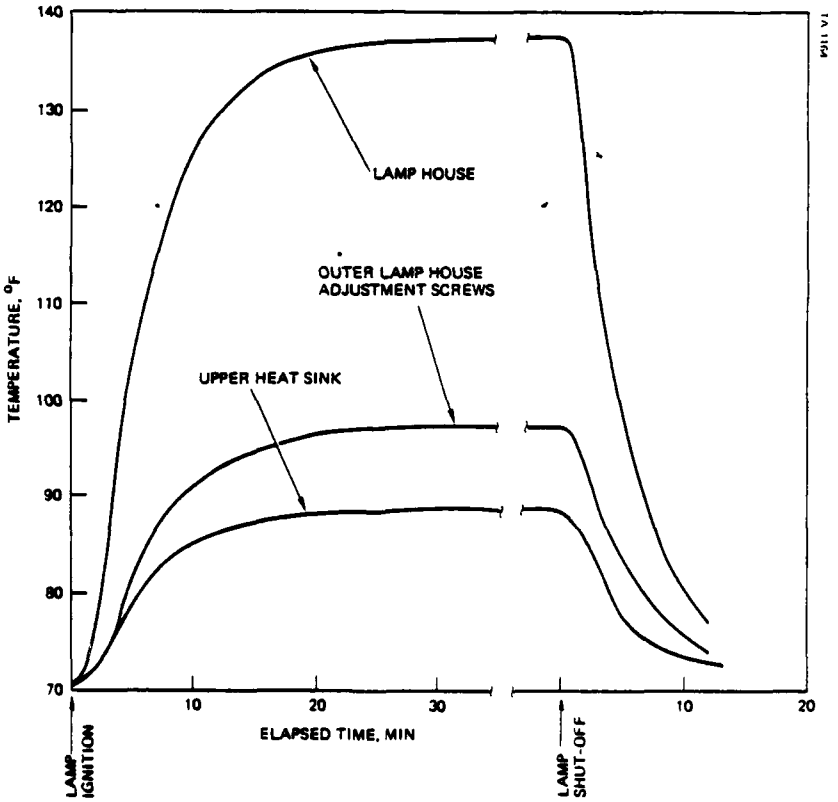


Figure 49. Lamp house temperature profile.

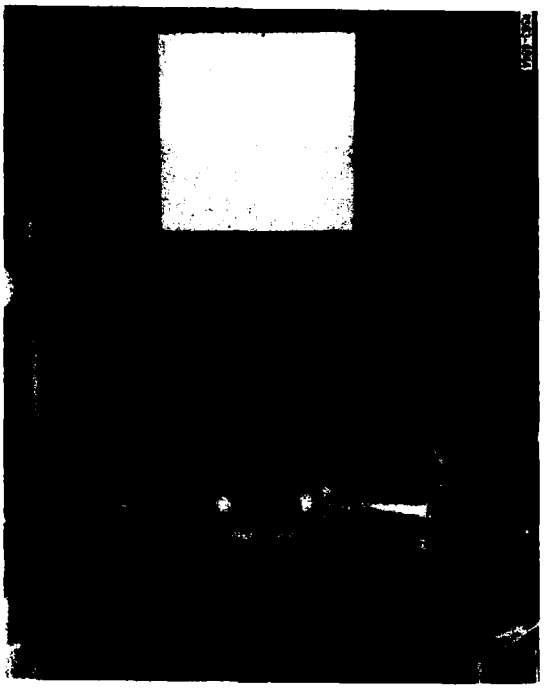


Figure 50. Screen/mirror assembly.

2. INTERFACE/DRIVE ELECTRONICS

The four module projection is not directly compatible with a standard television signal any more than a CRT without its associated electronics. The interface between the projection display and a composite video input is accomplished with control circuitry mounted in a card cage at the edge of the optical bench, LSI driver circuits mounted behind each of the four liquid crystal matrix display modules, three external laboratory power supplies, and the necessary interconnecting cables.

Control Circuitry

As illustrated in Figure 51, the inputs to the four module projection display consist of three power forms from external power supplies and a single 525-line composite video signal. The control circuitry simply converts the composite video signal into the levels and waveforms required by the LSI driver circuits, which are discussed in the next section. The control circuitry consists of a video amplifier with gamma correction, a synchronization pulse detector, timing logic and row drive power control circuitry.

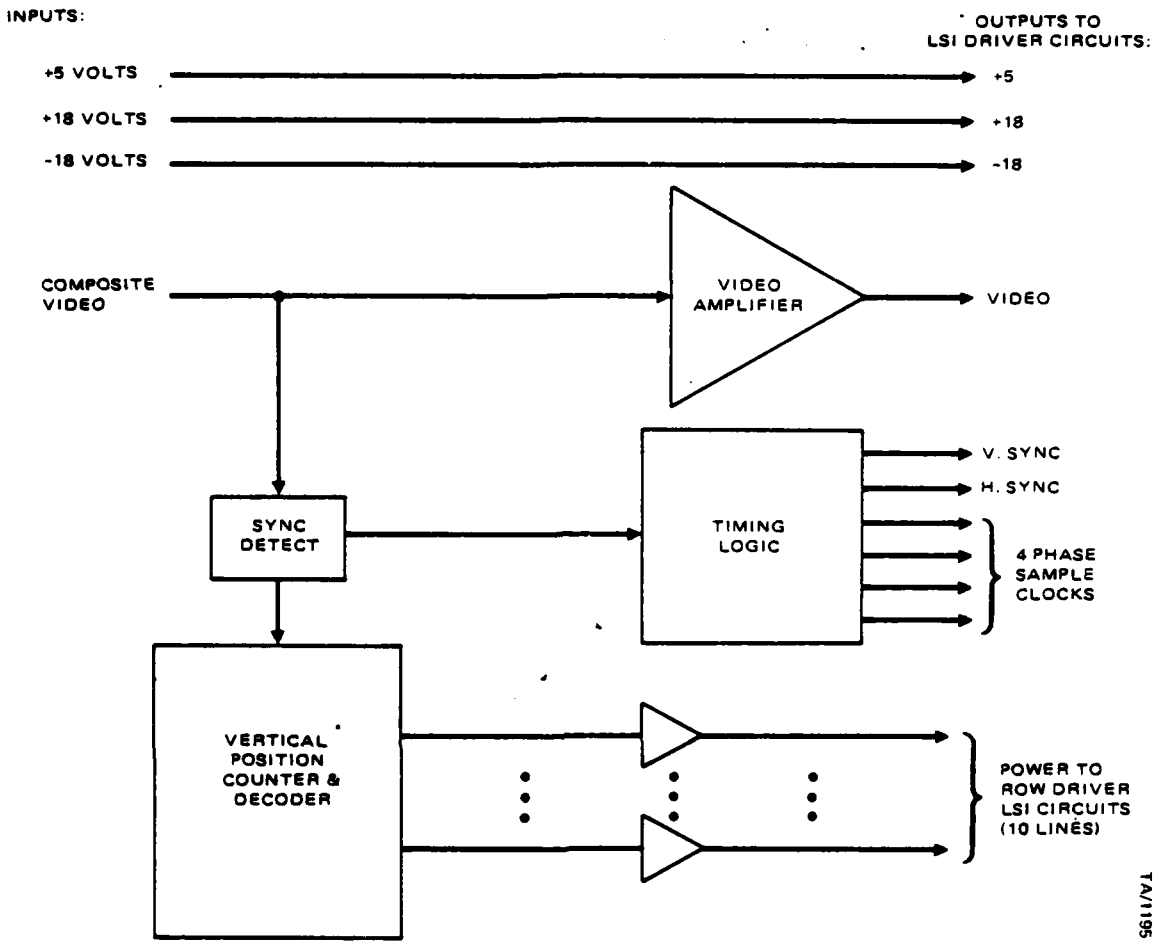


Figure 51. Control circuitry block diagram.

The row drive power control circuitry is used to reduce the power consumption of the LSI row drivers by controlling the power form applied to the amplifier stages in each LSI circuitry. The power is applied only during the time interval when a given LSI circuit is actively controlling its associated display module. Since the amplifier stages consume virtually all of the row drive power, and since each driver is active for only 35 of the 525 lines in the video image, this technique results in a considerable power savings.

The power consumption of the four-module projection display is summarized in Table 17. Of the 140-watt total consumption, 100 watts is used in the arc lamp, 8.5 watts in each of the four sets of driver circuit boards, and 6 watts in the control circuitry.

TABLE 17.

FOUR-MODULE PROJECTION DISPLAY POWER CONSUMPTION

Power Form Voltage (Volts)	Current (Amps)	Power Consumption (Watts)
+18	1.6	28.8
-18	0.45	8.1
+5	0.68	3.4
20 (lamp)	5.0	100.0
Total		140.3

As the 350x350-element resolution of the four module projection display does not conform to the 525-line video input on a one-to-one basis, a portion of the television picture is not shown. As illustrated schematically in Figure 52, only 175 lines of each television field are displayed. To preserve the 3:4 aspect ratio of the television image, each horizontal line is divided into 640 elements, of which 350 are displayed. These elements are sampled during a 28.4 microsecond interval of the 52 microsecond active line time, using a 12.3 megahertz clock. Vertical and horizontal position controls are provided such that the 350x350-element display "window" may be moved anywhere in the television image.

LSI Driver Circuits

Each of the four 175x175-element liquid crystal display modules requires 175 column (video) inputs and 175 row (sweep) inputs which are provided by custom column and row LSI driver circuits. The same LSI driver circuit designs were used on several previous programs. These circuits are mounted on printed wiring boards behind the display modules. The signals travel between the boards and the liquid crystal modules on flat Kapton cables, with each cable carrying 175 signals. Connections are made by soldering the cables to the printed wiring boards and by compressing the exposed conductors in the cable against corresponding electrode patterns on the display module substrate.

Redundant drive is provided to both ends of every row and column of the display modules. Conductor patterns on the display substrate provide a path for the column signals from the top of the module to the bottom. Two Kapton cables are soldered to each row driver circuit board; these cables are then clamped to the left and right sides of the display, respectively.

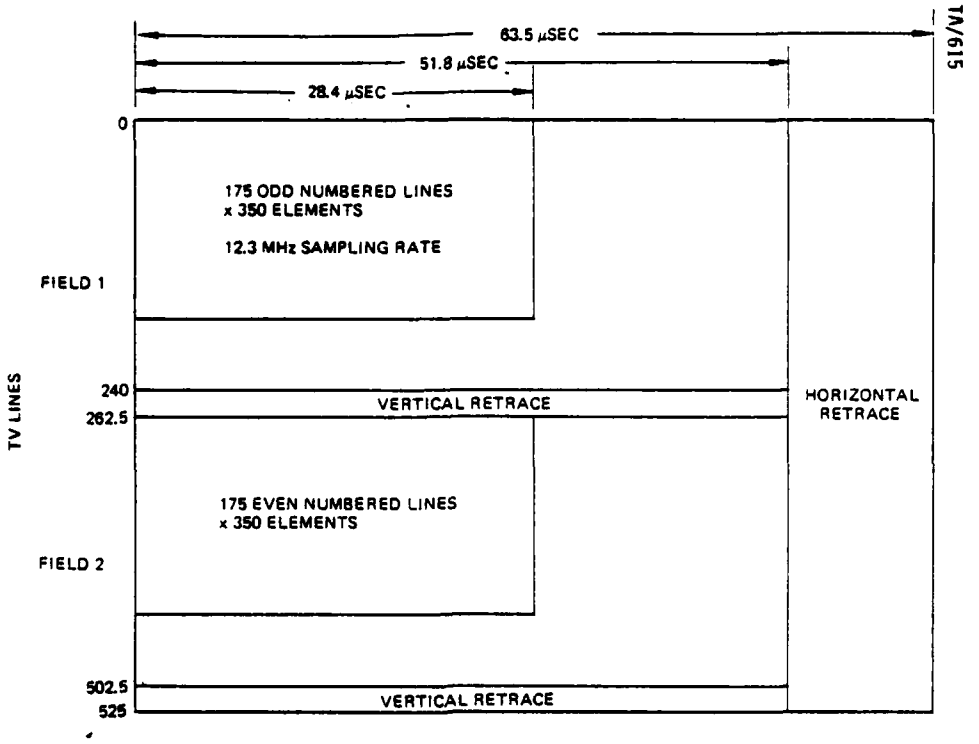


Figure 52. 525 line video sampling.

The row driver LSI circuit, as illustrated in Figure 53, is simply a thirty-five bit serial input shift register with thirty-five buffered parallel outputs. A delayed vertical sync pulse, shortened to one horizontal period in width, is applied to the enable-in input. The circuit is clocked by horizontal sync, and successive lines on the display are enabled as the enable-in pulse propagates from stage to stage in the shift register. When all 35 outputs from a given driver have been enabled, an enable-out signal propagates to the enable-in of the next circuit.

The interlace required for compatibility with a standard television input is accomplished using the timing shown in Figure 54. On the first line of field one, a single clock pulse is applied to enable the first row of the upper display modules. On successive lines, a double horizontal sync pulse is applied. Since the spacing between these pulse is short with respect to the response time of the buffer amplifiers, alternate outputs are skipped. The timing on field two is similar, except that a double horizontal sync pulse is applied on the first line.

Five row driver LSI circuits are mounted on a single printed wiring board having provisions for attaching two Kapton flat cables to drive both the left and right sides of a display module. Each LSI circuit has 35 outputs; thus one PWB can drive the 175 rows of a single display module.

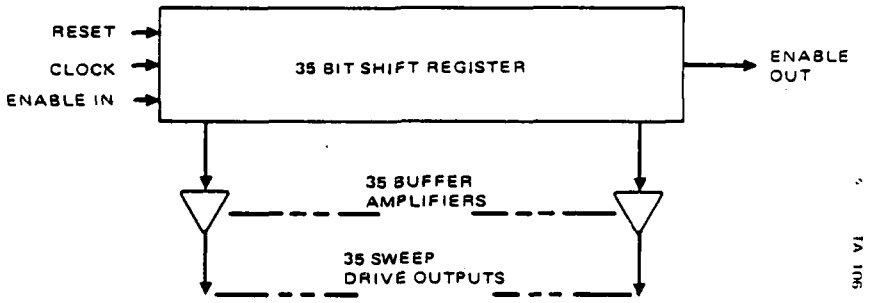


Figure 53. Row driver circuit block diagram.

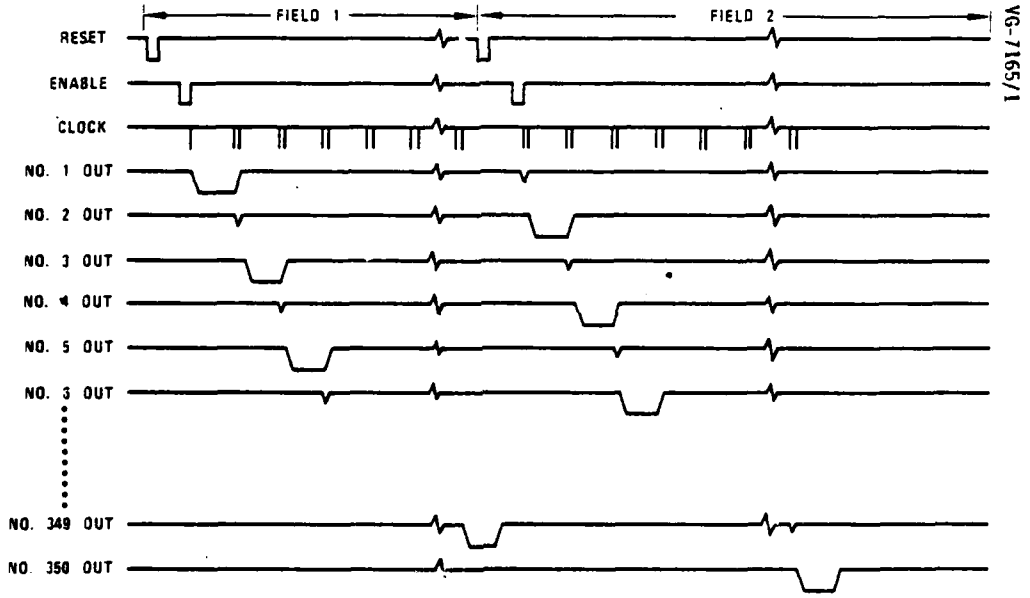


Figure 54. Sweep driver circuit timing.

As illustrated in Figure 55, the video driver circuit design can be divided into three functional areas. The shift register serves to propagate an enable signal such that the video samples for each column of the display are taken at sequential time intervals. The sampled data is stored in the form of charge on two banks of capacitors; one set of capacitors accumulates the samples for the current line while the second set outputs the samples for the previous line. Switching between the two banks is controlled by a single flip-flop which is toggled by the horizontal sync signal. The amplifiers provide both voltage amplification and impedance matching; their high input impedance prevents discharging the data storage capacitors while their low output impedance assures that the column electrode buses in the displays respond rapidly to signal changes.

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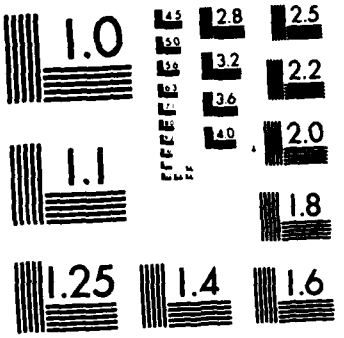

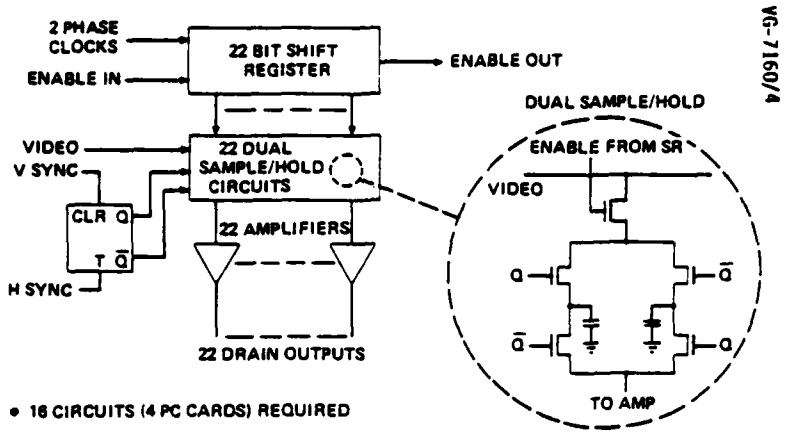

Figure 55. Column driver block diagram.

A troublesome feature of the column drive circuit chips is their interlaced sampling sequence. The chips are grouped together is sets of four, and they are driven by a four-phase clock such that first chip takes the first video sample, the second chip takes the second sample, etc., until the fifth video sample which is again taken by the first chip. A timing diagram for the video sampling in one driver chip is shown in Figure 56, and the output interlace required to place all video samples in the proper sequential order is shown in Figure 57.

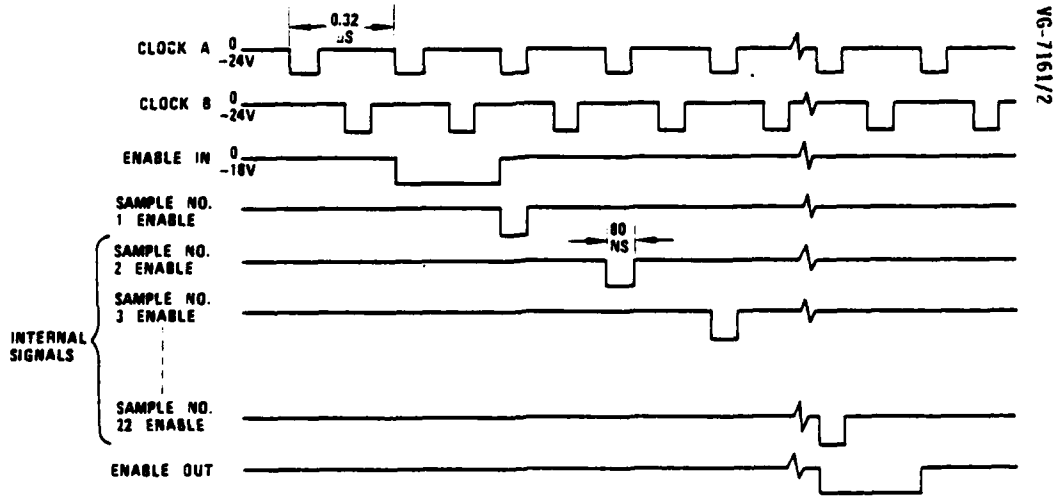

Figure 56. Column driver circuit timing.

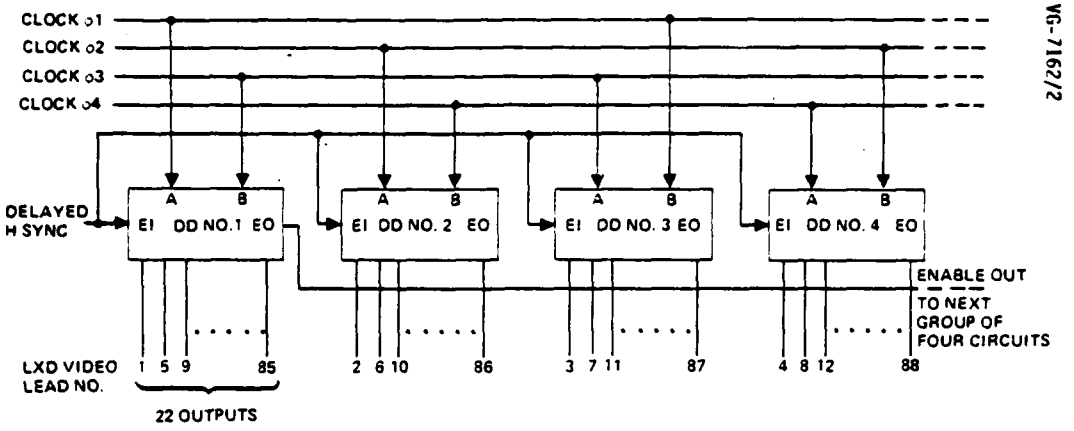

Figure 57. Column driver circuit interlace.

The interlaced sampling design was used to reduce the required shift register clock rate by a factor of four. One of the consequences of this design is that the voltage gains of the amplifiers in the four driver chips in an interlaced set must be very well matched or objectionable fixed pattern noise, which appears as a bar pattern that repeats every fourth column, will be added to the display imagery.

A total of 157 column driver LSI circuits were tested prior to assembly of the four module projection display. Of these, 62 had one or more nonfunctional outputs, and 13 had wide variations in voltage gain across their 22 outputs. These 13 drivers would be suitable for a non-video display. The input to output voltage transfer characteristics of the remaining 82 drivers were measured at five values of input voltage. Figure 58 shows the input/output characteristics of the two worst-match driver circuits.

A computer program was then used to sort the data and to match the drivers into four sets of 8 circuits. Figure 59 shows the input/output characteristics of the eight drivers in one matched set. Although the outputs of the drivers in a given set match within a few tenths of a volt, a limited amount of fixed pattern noise is still visible in most of the display photographs in this report.

An interlaced set of four column driver circuits is mounted on a printed wiring board along with two high speed sampling clock drivers. Two such boards are paired to drive a single 176-conductor Kapton cable which is split to allow 88 conductors to be soldered to each wiring board. One such cable/board assembly is required to drive each 175x175-element display module.

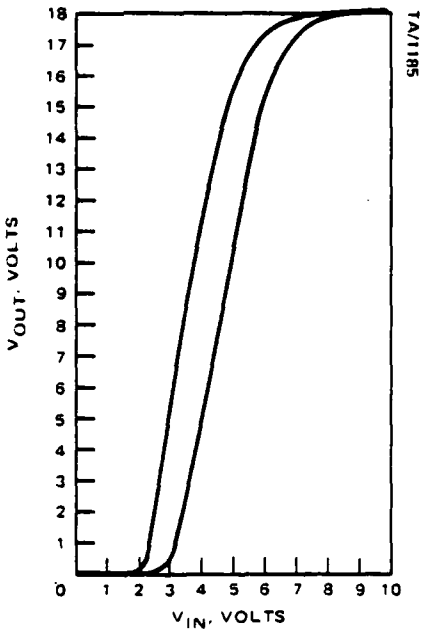

Figure 58. Worst case driver characteristics.

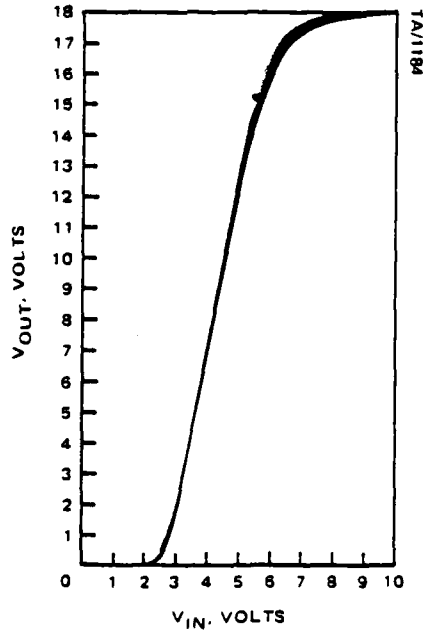

Figure 59. Characteristics of eight matched column driver LSI circuits.

One row driver board and a pair of column driver boards are mounted behind each of the four 175x175-element liquid crystal display modules in the projection display. A fourth circuit board functions to terminate the cable between each display assembly and the control circuitry, and to distribute the control signals to the three LSI driver boards.

3. FOUR MODULE PROJECTION DISPLAY PERFORMANCE

A series of performance measurements were made on the completed four module projection display. The parameters measured included brightness and contrast, physical alignment of the four image quadrants, and intensity of spurious reflections.

Brightness and Contrast

The brightness and contrast of the optical bench Quad were measured at 36 points (nine per quadrant) to determine the overall uniformity of the display. Table 18 lists the measured contrast and the brightness as a function of screen position.

The average brightness of the screen, with the four section Fresnel field lens in place, was 3870 foot-Lamberts with standard deviation of 420 foot-Lamberts. The peak brightness was 5000 foot-Lamberts. The brightness exhibited by a ground glass screen without fresnel lenses was also measured. In this case the peak brightness was greater at 5380 foot-Lamberts, but the average brightness was only 1500 foot-Lamberts. The standard deviation of the brightness without the fresnel lenses was 1320 foot-Lamberts.

Alignment

The alignment of two images was measured in two parts: longitudinal and transverse. Longitudinal alignment refers to the gap between the two images caused by a combination of the image separation and the shadow of the gap between the fresnel lenses. Transverse alignment refers to the amount of shear between two images. Transverse alignment errors will cause a straight line running through the gap to step to one side and appear discontinuous. This type of mis-alignment can be caused by differing magnification factors between the two images.

Both types of alignment were measured on the four module projection display. The transverse alignment was measured repeatedly during the procedure to align the four images. With a video image of a box displayed at the screen, the four images were brought into alignment relative to one another and the position of the fresnel lenses. The image of the box was then moved by way of the horizontal and vertical positioning knobs to check the alignment everywhere along each gap. The magnification of the four quadrants of the image was adjusted until the traverse alignment was small and consistent along the four gaps. The transverse alignment was held to less than one-half of a picture element anywhere along the gaps.

TABLE 18.

BRIGHTNESS AND CONTRAST OF FOUR MODULE PROJECTION DISPLAY

Upper Left			Upper Right		
3540	3440	3380	3770	4070	3580
19.3	17.7	10.4	17.3	2.5	16.0
4030	4480	4010	4490	5000	3630
21.0	16.3	12.6	15.2	1.8	12.7
4060	4160	3940	3350	4200	3670
20.8	17.7	16.5	14.8	2.9	16.9
Lower Left			**Lower Right**		
3450	3620	3270	3370	3870	4000
15.1	14.4	17.0	22.8	17.1	12.0
3650	3950	3340	4000	4410	4310
17.1	14.5	16.0	23.1	12.3	9.4
3160	3820	3570	4060	4510	4090
24.0	22.1	18.8	25.5	21.2	11.1

Notes: 1. Brightness (upper number) and contrast (lower number) measured at 36 points.

2. Position in table corresponds to approximate position on projected image.

Longitudinal alignment could not be completely eliminated by adjustment. Since the fresnel field lens structure was composed of four discrete lenses, a small gap between the adjacent lenses was inevitable. The gaps appear as a dark line on the screen. Under microscopic investigation, the edges of the fresnel lenses showed the signs of sawing with small cracks and chips. Nevertheless, the gaps did not hinder the readability of information extending across two quadrants of the display.

A microscanning photometer was used to measure the amount of the longitudinal misalignment. Figure 60 shows a plot of brightness versus distance relative to the center of the gap between two image quadrants. The brightness of the gap is at least a tenth of the display brightness; the gap width is about 10 mils (full width at half maximum). Therefore, the size of the gap is on the order of a half of a picture element. If the Quad fresnel lens had been manufactured as a single unit (with the metal molds being fixed

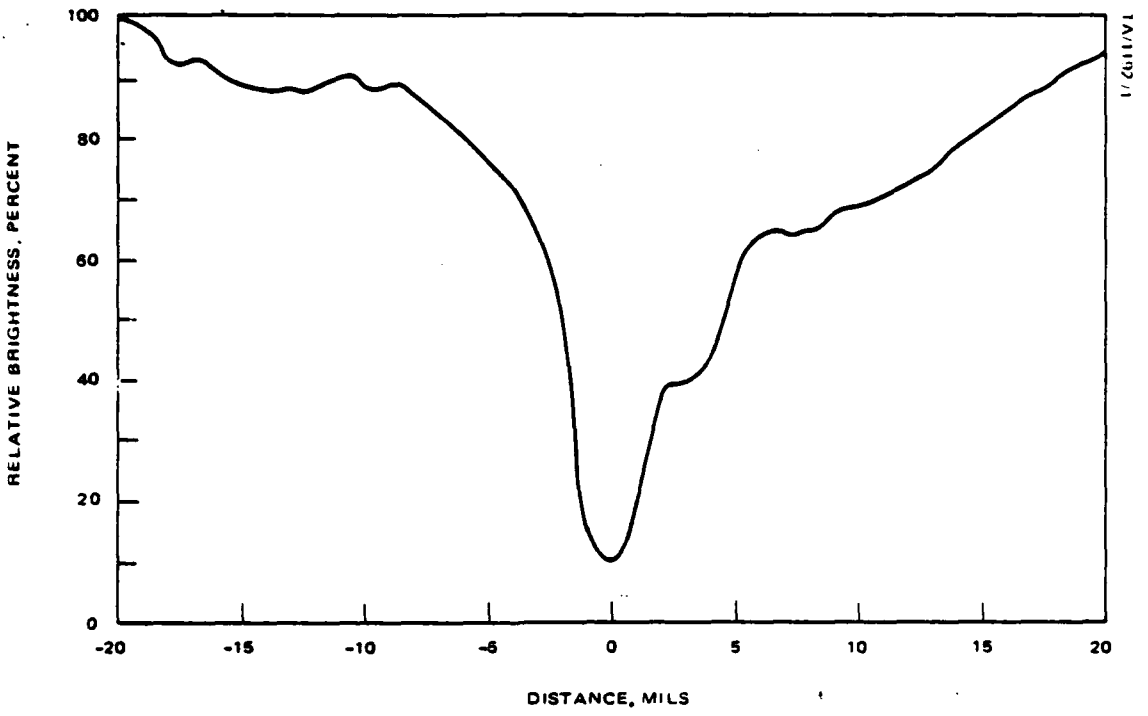

Figure 60. Display brightness across the gap between two image quadrants.

together before the pressing of the lenses), the gap could be reduced to zero, assuming that the images have enough adjustment for proper alignment.

Spurious Reflections

In any projection system, spurious reflections from the surfaces of uncoated lenses can make their way to the screen to degrade contrast or produce areas of brightness non-uniformity. To minimize these spurious reflections, the projection optics in the four module projection display were well coated and the display contrast was not limited by spurious reflections. However, the condensing optics were not coated, since it was believed that reflections from the condensing lenses would not effect display performance. This belief was in error, and noticeable rings were displayed within each quadrant. These rings resulted from nonuniform illumination of the liquid crystal modules due to multiple reflections within the condensing optical system. Future designs would require the coating of all lenses. Photographs of images on the four module projection display are shown in Figure 61.

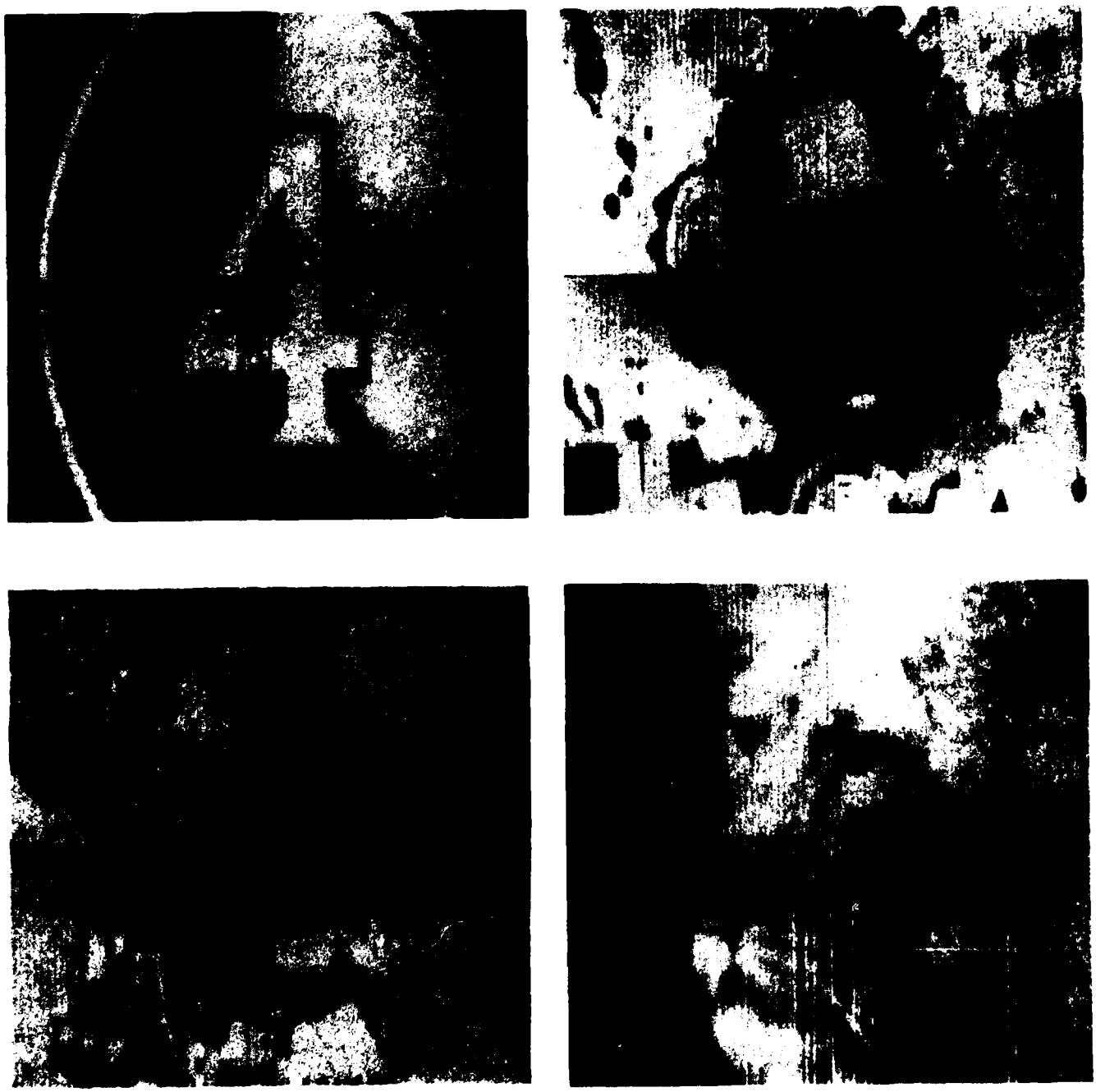

Figure 61. Images on the four module projection display.

SECTION VI.

CONCLUSIONS AND RECOMMENDATIONS

The objectives of the Head-Up Display Technology Demonstration Program were to improve the quality of the liquid crystal matrix display modules and to demonstrate an optical projection technique to combine the images from multiple, physically separate, display modules into a continuous high resolution display surface. Both of these objectives were essentially accomplished during the course of the program.

An improved process for depositing optical quality mirrors on the display matrix circuit resulted in display devices with 50% higher reflectivity, in a projection system, than the devices fabricated on previous programs. Additionally, the liquid crystal displays fabricated on this program incorporated a low reflectivity multi-layer transparent electrode. The net effect of these two improvements was an increase in projection display contrast by a factor of over two to one.

Improved silicon processing procedures developed during this program resulted in a decrease in the average number of line defects in the matrix circuits. Additionally, several process procedures were investigated, but not fully developed, which have the potential for an even greater improvement in future programs. The number of defects in the display devices was also reduced by improved wafer testing procedures, redundant drive to the display devices, and repair of some types of faults.

An optical projection technique for combining the images from multiple liquid crystal display modules was conceived and demonstrated in an optical bench model. In this model, the images from four 175x175-element liquid crystal modules were projected in juxtaposition on a common screen to form a continuous, 7x7-inch, 350x350-element, image. The raster brightness of this display was 4000 foot-Lamberts, the contrast ratio exceeded 18:1, and the power consumption was less than 150 watts.

The results achieved on this program lead directly to four major conclusions:

1. The optical performance of the matrix liquid crystal display modules can exceed, by far, any realistic display requirements. The contrast ratio of the optical bench model projection display constructed on this program was limited by the projection optical system. The contrast ratio of the liquid crystal display modules, measured in a test set representative of an optimal projection system, regularly exceeded 50:1 and, in many cases, 100:1.

2. An acceptable yield of defect-free display matrix circuits can be achieved, particularly if the size of the matrix circuit is reduced. Although the yield of defect-free devices constructed on this program was not high, a significant improvement was made. Additionally, the investigation of several alternative silicon wafer fabrication processes, each of which has the potential to significantly reduce defects, was started. Many of the silicon wafers processed on this program had one or two defective lines; assuming that the area of the circuit was reduced to 25% of that of the current device, each of these wafers would have contained one or two perfect devices.

3. Optical projection techniques can be used to combine the images from multiple liquid crystal modules without objectionable image discontinuities or loss of information. The gaps between the four quadrants of the optical bench model constructed on this program were less than one-half picture element in width. These gaps were caused by physical cracks in the projection screen structure, rather than by difficiencies in the projection optics. This development can lead to a truly modular display architechture in which a single liquid crystal/optics module can be replicated and used to construct displays of any size and resolution.

4. The combination of matrix liquid crystal display modules and optical projection techniques can provide a combination of display viewing area, brightness, contrast, and power consumption that can not be achieved with any other known display technology. The raster brightness of the optical bench four-module projection display constructed on this program is greater than that of a CRT of equal size by a factor of two, and orders of magnitude greater than that of flat-panel matrix displays. Additionally, the brightness of the projection display model could have been increased by nearly 40% simply by using antireflection coatings on the condensing optics.

The results achieved on this program and the four-module projection display demonstration unit have three deficiencies which must be noted. First, the 350x350-element resolution of the model projection display, although adequate for many applications, is not sufficient to display the imagery from future airborne radar and infrared sensors. Second, the physical size of the display model is much larger than the volume available for cockpit displays. Third, although the significant improvements made on this program indicate a potential for high yield, improvements in the yield of the display modules is required. All three of these problem areas can be reduced in future programs if a smaller, higher resolution, liquid crystal display device is used.

A 240x320-element, 0.75x1.0-inch, 320-element-per-inch, liquid crystal display module is currently being developed on a company-sponsored effort. This device has the following advantages over the 175x175-element display modules constructed during the Head-Up Display Technology Demonstration Program.

a. The small size of the 240x320-element display module allows four of the matrix circuits to be fabricated on a single 3-inch silicon wafer. Thus the silicon processing costs for this device are one-fourth of those for the larger 175x175-element display.

b. The small size of the 240x320-element device results in higher yields of good matrix circuits. Although this device has had several years less development than the 175x175-element display, its yields are already much higher.

c. The smaller display device obviously provides higher resolution per liquid crystal module. In particular, four of the 240x320-element displays can be combined to provide a full-resolution 525-line video display.

d. The size of the optics required to project an image from the 240x320-element display module is much smaller than that of the optics used in the demonstration display constructed on this program. A 5x7-inch viewing area, four-module, projection display using the smaller liquid crystal module would have a depth of less than 10 inches.

Thus the efforts on the Head-Up Display Technology Demonstration Program lead to three major conclusions. First, since the combination of liquid crystal and projection optical technologies has the potential to provide display performance that can not be obtained with any other technologies, the development of this technology should be continued for both Head-Up and Head-Down displays. Second, the 240x320-element display module should be used in any new programs, instead of the 175x175-element display. Third, given the major advantages of increasing the resolution element density in the display matrix, a study of the feasibility of constructing even higher resolution modules should be performed.

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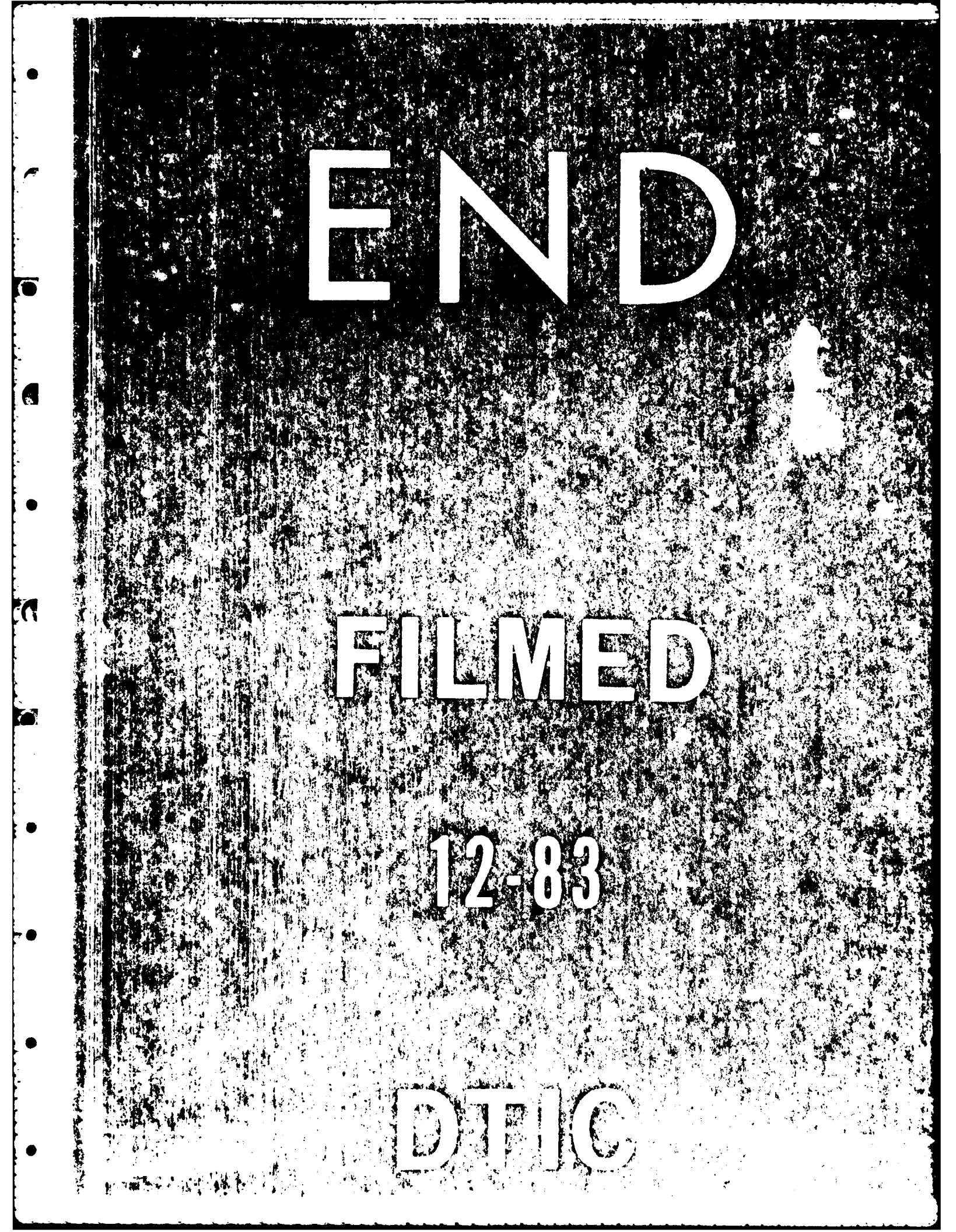
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